1 Before you begin

In this laboratory you will design and implement a washing machine controller as originally conceived by Mano and Kime.

You are required to construct an algorithmic state machine (ASM) representation for the washer control unit from a given specification. The ASM chart is then to be converted into a state table and implemented as a behavioural VHDL model. The datapath of the controller consists of a variable timer that is to be specified using a combination of structural and behavioural design styles. The lab involves submitting your preparatory work and laboratory results in the form of a neatly presented, original assignment, and will require you to demonstrate your implementation.

Laboratory Exercise 5 is scheduled to run for three weeks. Various tasks need to be completed and submitted at different times as you proceed to its completion. Before commencing work in the laboratory, you are expected to complete and submit the design of your controller as part of Assignment 2. You will then implement and verify your design during the laboratory time and demonstrate your final implementation. At the completion of the lab, you are required to submit the second part of Assignment 2 comprising the VHDL code and simulation waveforms you obtained in the course of the lab. Please note that it is important to meet all deadlines in order to avoid losing marks.

2 Assignment 2 (40 marks)

Assignment 2 consists of two parts. Part I comprises the preparatory exercises for this lab (see Section 4.1 below). You are required to hand in a neatly prepared, original submission for Part I at the beginning of your lab session in Week 12. Note: messy work will attract a 2 mark penalty and assignments containing copied work will be given a zero mark. This part will be marked by your lab demonstrator and returned to you as soon as possible. Since this part of the assignment contains the designs for the circuits you will implement, you should make a copy of your work prior to handing it in. Part I is worth 20 marks. If Part I is not handed in before the end of your lab session in Week 12, you will lose 5 marks. If it is not handed in by the end of your lab session in Week 13, it will not be assessed.

Part II of the Assignment consists of a compilation of the code and simulation waveforms you prepared during the course of the laboratory (see Section 4.2 below). This part is worth 20 marks, and should be submitted by the end of your lab session in Week 14. If you do not hand in Part II prior to the end of your lab session in Week 14, you will be penalized 5 marks. Part II of Assignment 2 will not be accepted for marking after Week 15.

3 Demonstration (5 marks)

You are required to demonstrate your simulation of the completed washing machine controller by the end of your lab session in Week 14. You will also need to be able to answer questions on the design you implemented. Since the demonstrations are expected to take some time, and it will not be possible for you to demonstrate your work after Week 14, you are strongly encouraged to complete your demonstration as soon as possible.

4 Washing Machine Controller Specification

Adapted from Mano & Kime, 3rd Ed., Problem 8-6.
The ASM chart for a synchronous washing machine controller with clock CLK and asynchronous RESET is to be developed. The circuit has three external inputs, START, FULL, and EMPTY (which are 1 for at most a single clock cycle and are mutually exclusive), and external outputs, HOT, COLD, DRAIN, and TURN. The datapath for the control consists of a 4-bit synchronous down-counter, logic to control the value to be loaded into the counter, and an output, ZERO, which is 1 whenever the counter contains value zero and is 0 otherwise. The datapath has synchronous LOAD and DEC and asynchronous RESET inputs to control the counter. The counter synchronously decrements once each clock cycle for DEC = 1 and can be loaded on any cycle of clock CLK. An additional 2-bit input, SEL, and 4-bit input, TIME, determine the initial value loaded into the counter.

In its operation, the circuit goes through four distinct cycles, WASH, SPIN, RINSE, and SPIN, which are detailed as follows:

WASH: Assume that the circuit is in its power-up state IDLE. If START is 1 for a clock cycle, HOT becomes 1 and remains 1 until FULL = 1, filling the washer with hot water. Next, using LOAD, the down-counter is loaded with the value TIME from a panel dial which indicates how many clock cycles the wash cycle is to last. DEC and TURN then become 1 and the washer washes its contents. When ZERO becomes 1, the wash is complete, and TURN and DEC become 0.

SPIN: Next, DRAIN becomes 1, draining the wash water. When EMPTY becomes 1, the down-counter is loaded with 7. DEC and TURN then become 1 and the remaining wash water is wrung from the contents. When ZERO becomes 1, the wash is complete, and DRAIN, DEC, and TURN return to 0.

RINSE: Next, COLD becomes 1 and remains 1 until FULL = 1, filling the washer with cold rinse water. Next, using LOAD, the down-counter is loaded with value 10. DEC and TURN then become 1 and the washer rinses its contents. When ZERO becomes 1, the rinse is complete, and TURN and DEC become 0.

SPIN: Next, DRAIN becomes 1, draining the rinse water. When EMPTY becomes 1, the down-counter is loaded with 8. DEC and TURN then become 1 and the remaining rinse water is wrung from the contents. When ZERO becomes 1, DRAIN, DEC, and TURN return to 0 and the circuit returns to state IDLE.

4.1 Assignment 2 Part I – Preparation (due by Lab Session start, Week 12: 20 marks)

1. Derive the ASM chart for the washing machine controller. Assign meaningful state names to each state box. (8 marks)

2. Construct a state table corresponding to the ASM chart you derived. Include the next state and outputs for each present state and input combination. (4 marks)

3. Partition the washing machine controller into Control Unit and Datapath modules as illustrated in the diagram of Figure 1. Draft a copy of the diagram clearly identifying, by the names given in the specification above, the control inputs, control outputs, control signals, status signals, data inputs, and data outputs used in the design of the washing machine controller. (2 marks)

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Figure 1: High-level decomposition of a digital system
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4. Elaborate the structure of the datapath by drafting a refined copy of the module. (4 marks)
   a) Include all inputs and outputs identified in part 4.1.3 above.
   b) Within the datapath box include a block for the 4-bit down-counter with ENABLE, LOAD, and RESET inputs.
   c) Illustrate the logic needed to produce the ZERO output.
d) Identify the logic needed to select the correct value to load into the down-counter (wash-time select logic).
e) Show how these sub-modules are interconnected.

5. Develop a gate-level design of the 4-bit synchronous down-counter with ENABLE, LOAD, and asynchronous RESET inputs using positive edge-triggered D-type flip-flops with asynchronous resets as fundamental components. Reference all sources used in the design. (2 marks)

4.2 Assignment 2 Part II – Laboratory Report (due by Lab Session end, Week 14: 20 marks)

1. Specify and test a 3-process behavioural VHDL model of the Control Unit.
a) Define processes for the next state, output, and clock (state update) functions of the washing machine Control Unit.
b) Design a set of test waveforms to verify the correct operation of the Control Unit. Print a copy of your test input and output waveforms for inclusion in your laboratory report. (6 marks)

2. Implement and suitably test a structural VHDL model of your down-counter design from 4.1.5 above. You may use a behavioural implementation of a D-type flip-flop with asynchronous reset as a component. Print a copy of your test input and output waveforms for inclusion in your laboratory report. (6 marks)

3. Implement and test a behavioural VHDL (process) model of your wash-time select logic as identified in 4.1.4 above.

4. Implement and thoroughly test a VHDL implementation of the Datapath you designed in 4.1.4. Print a copy of your test input and output waveforms for inclusion in your laboratory report. (5 marks)

5. Integrate your models of the Control Unit and Datapath from 4.2.1 and 4.2.4. Develop an appropriate set of test vectors and verify the correctness of your design. Print a copy of your test input and output waveforms for inclusion in your laboratory report. (3 marks)

4.3 Demonstration (Due by Lab Session end, Week 14: 5 marks)

1. Demonstrate the simulation of the VHDL description of your washing machine controller. Be prepared for any questions your demonstrator may ask of you.

5 Bonuses

This section specifies bonus problems that should not be attempted until you have completed the Assignment and Lab as defined in Section 4 above. Please feel free to attempt the following problems if you have completed the above components and like a challenge. You need not complete 5.1 before attempting 5.2. You do not need to attempt or finish either component. The maximum number of bonus marks possible is 21.

5.1 One-hot Control Unit Implementation (6 marks)

Derive a one-hot (single flip-flop per state) encoding of the control unit logic and implement.

1. Include a logic diagram of your implementation in Assignment 2 Part II (3 marks)
2. Include your VHDL code and simulation results in Assignment 2 Part II (3 marks)

5.2 Programmable Washing Machine Controller (15 marks)

Develop a programmable version of the washing machine controller as illustrated in Figure 2. This version of the controller uses the program counter (PC) to retrieve instructions from program memory. The PC can be asynchronously cleared to point to the instruction at memory location 0 by asserting RESET. The instruction referenced by the program counter is decoded to produce the control signals for the datapath and condition
codes for the conditional PC increment logic. This logic produces an INC signal whenever the PC is to be incremented to point to the next instruction in memory. In order to produce the INC signal the conditional PC increment logic also relies on the external inputs (FULL, EMPTY, START) and datapath status signal (ZERO) as before. When the input corresponding to the condition being waited upon is asserted, the INC signal is set to 1, otherwise INC = 0. Include a design of your controller in Assignment 2 Part II.

![Figure 2: Programmable control unit](image)

**Figure 2: Programmable control unit**

a) Identify the set of unique operations performed by the controller. When are they active? What are the control signals that must be produced? (2 marks)

b) Define a suitable (nice and minimal) instruction set by devising an encoding for each of the unique operations performed by the controller. In particular, you should include two LOAD instructions for the counter: a LOAD TIME instruction to load the value given by the panel dial value, TIME, and a LOAD <immediate> instruction to load a 4-bit immediate value given by the instruction. The datapath can thus be modified to simplify the wash-time select logic. (3 marks)

c) Identify the condition codes needed by the conditional PC increment logic and define the logic needed to produce the INC signal. (2 marks)

d) Determine the decoder logic needed to produce the control signals. (2 marks)

Implement and test your programmable controller and datapath in VHDL. Demonstrate your design to your demonstrator. Include a copy of your code and test waveforms in Assignment 2 Part II (6 marks).

6 A final word on marks

The course outline allocated 10 marks to Assignment 2 and 5 marks to Lab 5, for a total of 15 marks of your final assessment. The marks listed in Section 4 of this specification will therefore need to be scaled to 15. This will be achieved by dividing your total mark for Section 4 by 3 and distributing these marks in the ratio 2:1 for your Assignment 2 and Lab 5 marks.

Any bonus marks awarded will also be divided by 3 and added to your final result for COMP2021 to a maximum possible total score of 100.