

## Hardware-Assisted Critical Sections

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## Where we are at

In the last lecture we introduced efficient algorithms for critical section solutions for  $N$  processes.

In this lecture, we will talk more about **hardware-assisted** critical sections and how they are used to implement a basic unit of synchronisation, called a *lock* or *mutex*.

# Machine Instructions

Recall the **exchange** solution:

bit common $\leftarrow 1$	
bit tp $\leftarrow 0$	bit tq $\leftarrow 0$
<b>forever do</b>	<b>forever do</b>
p <sub>1</sub> <i>non-critical section</i>	q <sub>1</sub> <i>non-critical section</i>
<b>repeat</b>	<b>repeat</b>
p <sub>2</sub> XC(tp, common)	q <sub>2</sub> XC(tq, common);
p <sub>3</sub> <b>until</b> tp = 1	q <sub>3</sub> <b>until</b> tq = 1
p <sub>4</sub> <b>critical section</b>	q <sub>4</sub> <b>critical section</b>
p <sub>5</sub> XC(tp, common)	q <sub>5</sub> XC(tq, common)

# Machine Instructions

Now let's see the **test and set** solution:

$$\text{TS}(x, y) \equiv x, y := y, 1 \text{ (atomically)}$$

bit common $\leftarrow$ 0	
bit tp	bit tq
<b>forever do</b>	<b>forever do</b>
p <sub>1</sub> <i>non-critical section</i>	q <sub>1</sub> <i>non-critical section</i>
<b>repeat</b>	<b>repeat</b>
p <sub>2</sub> TS(tp, common)	q <sub>2</sub> TS(tq, common);
p <sub>3</sub> <b>until</b> tp = 0	q <sub>3</sub> <b>until</b> tq = 0
p <sub>4</sub> <b>critical section</b>	q <sub>4</sub> <b>critical section</b>
p <sub>5</sub> common $\leftarrow$ 0	q <sub>5</sub> common $\leftarrow$ 0

## Locks

The variable *common* is called a *lock* (or *mutex*). A lock is the most common means of concurrency control in a programming language implementation. Typically it is abstracted into an abstract data type, with two operations:

- *Taking* the lock — the first exchange (step  $p_2/q_2$ )
- *Releasing* the lock — the second exchange (step  $p_5/q_5$ )

var lock	
<b>forever do</b>	<b>forever do</b>
$p_1$ <i>non-critical section</i>	$q_1$ <i>non-critical section</i>
$p_2$ <b>take</b> ( <i>lock</i> )	$q_2$ <b>take</b> ( <i>lock</i> );
$p_3$ <b>critical section</b>	$q_3$ <b>critical section</b>
$p_4$ <b>release</b> ( <i>lock</i> )	$q_4$ <b>release</b> ( <i>lock</i> );



## Architectural Problems

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Each processor must now consult main memory when reading in order to get an up-to-date value.



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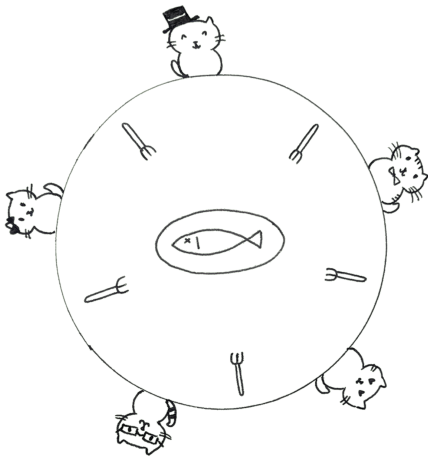
### With these instructions...

The processes spin while waiting, **writing to shared variables** on each spin. This quickly causes the bus to become **jammed**, and can delay processes from releasing the lock (c.f. the *thundering herd* problem).

## The solution?

Johannes will demonstrate in Promela the **test-and-test-and-set** solution (and a similar approach for exchange).

## Dining Philosophers



Five philosophers sit around a dining table with a huge bowl of spaghetti in the centre, five plates, and five forks, all laid out evenly. For whatever reason, philosophers can eat spaghetti only with **two** forks<sup>a</sup>. The philosophers would like to alternate between eating and thinking.

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<sup>a</sup>This would be more convincing with chopsticks. Blame Tony Hoare.

## Looks like Critical Sections

**forever do**

*think*

*pre-protocol*

*eat*

*post-protocol*

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For philosopher  $i \in 0 \dots 4$ :

$f_0, f_1, f_2, f_3, f_4$

**forever do**

*think*

**take**( $f_i$ )

**take**( $f_{(i+1) \bmod 5}$ )

*eat*

**release**( $f_i$ )

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**Deadlock** is possible (consider lockstep).

## Fixing the Issue

$f_0, f_1, f_2, f_3, f_4$	
Philosophers 0..3	Philosopher 4
<b>forever do</b> <i>think</i> <b>take</b> ( $f_i$ ) <b>take</b> ( $f_{(i+1) \bmod 5}$ ) <i>eat</i> <b>release</b> ( $f_i$ ) <b>release</b> ( $f_{(i+1) \bmod 5}$ )	<b>forever do</b> <i>think</i> <b>take</b> ( $f_0$ ) <b>take</b> ( $f_4$ ) <i>eat</i> <b>release</b> ( $f_0$ ) <b>release</b> ( $f_4$ )



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We have to enforce a **global ordering** of locks.

## What now?

- Assignment 0 deadline is on Monday.
- Assignment 1 comes out next week! Please find a **partner!**
- Next week: We will look at **semaphores** and **monitors**.