

COMP3211/9211 Computer Architecture 2011 Project

Encryption/Tagging Processor Design

Part 3 Multi-Processor (Optional)

This part is an extension of the project design and is designed to be completed by **individuals**. It is not compulsory; however, if you complete it and demonstrate your work by week 13, you will be awarded up to 5 marks (yes, no scaling, whatever you got will be added to your final results).

Problem Overview

Refer to the specification of Project Part 1 for the description of the encryption/Tagging problem.

Task Specification

Based on your design project part 1 or project part 2, construct a 2-processor system for parallel encryption/tagging a long plaintext string. To simplify the design, you can assume the two processors have their own instruction memory but share a data memory, as illustrated in Figure 1.

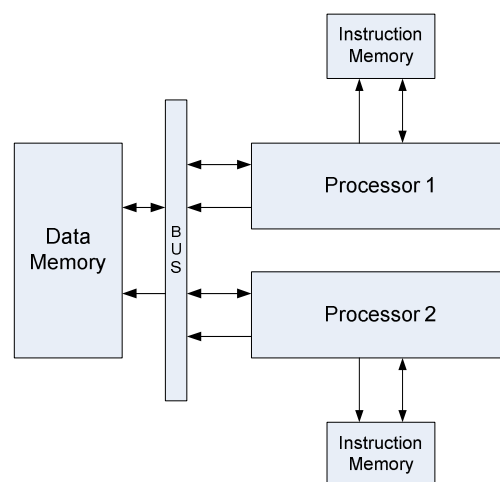


Figure 1: Multi-Processor

Both processors execute in parallel. Each processor performs encryption and tagging for different section of the plaintext in the data memory.

Assume the data memory has single port. Only one processor can access the data memory each time. We also assume the instruction memory has the same speed of the

processor but the data memory requires 5 clock cycles for each access.

You need to design how memory is accessed by the two processors in order to complete the encryption and tagging as quickly as possible.

Deliverables:

- Electronic copy of VHDL source code for the design
- A report (up to 5 pages) that provides
 - A brief description of your design.
 - A short discussion of your design strategy and techniques
 - VHDL testing waveform to demonstrate your design.
- Demonstration

A system will be set up for the electronic submission (due on Sunday, June 5, 2011). The demonstration will be run in week 13.