Goal: Project work. Ensure all aspects of the presentation are covered.

Questions: Consider the inner loop (C language level) of the MATDIFF processor.

1. What is a line-by-line translation into the instruction set you have created?

2. What critical changes have you made to the Single Cycle Core in order to implement the instruction set for the inner loop?

3. What is the critical path delay of your implementation?

   [Hint: the critical path delay of the Single Cycle Core is 8 ns, assuming the latencies as specified for MATDIFF are used. The period corresponding to this delay is 16 ns. Why? Can the period be reduced to 8 ns? What changes would need to be made to the core?]

4. What modifications to the VHDL code are needed to include the delays for components as specified for the MATDIFF project?

   [Hint: Any VHDL assignment can have an “…after {real number} {units of time}” clause added to it. For example, the statement

   \[
   a \leq b \text{ after } 5 \text{ ns};
   \]

   assigns the value b to a after a delay of 5 ns. Clearly, such clauses are non-synthesizable, but they are very useful in simulating the estimated delays of a subcomponent were it implemented in its target hardware.]