

COMP3211/9211 11s1

Tutorial 2 (Week 03)

1. Explain how the MIPS ISA embodies the following design principles:
 - a) simplicity favours regularity, and
 - b) compromise to achieve good design

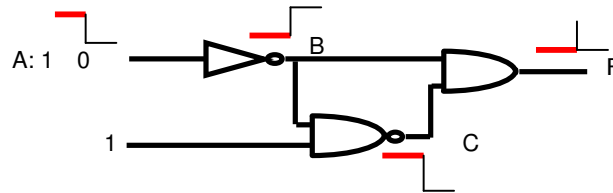
2. Suppose your program needs to read a word at memory address 0x12345678. Explain what sequence of MIPS instructions need to be executed to load the required word into R2 assuming R1 is available to store the address.

3. Considering the slide 22 of wk1_2 on the Single Cycle Processor Design, assuming
 - register/memory set-up times are 0.5 ns,
 - the propagation delay (clock-to-Q) of a flip-flop (register) is 0.5 ns,
 - the memory access time is 5 ns,
 - the delay of the control path (decoder) is 0.5 ns,
 - the register file access delay is 1 ns,
 - the delay of a MUX is 0.5 ns,
 - the delay of a zero or sign extender is 0.1 ns,
 - the delay of an ALU is 2 ns, and
 - the delay of an adder is 1.5 ns,
 - (a) Sketch a timing diagram, such as in slide 16, for a load instruction.
 - (b) Which of the load, store, add, and branch instructions is the one that requires the longest clock period?
 - (c) What is the minimum clock time assuming register/memory hold times are relatively very small and can be ignored?

4. How would you implement the jump instruction into the single cycle processor discussed in weeks 1-2 (refer slide 21 of wk2_1)?

5. Find the shortest sequence of MIPS instructions to determine the absolute value of a two's complement integer. Convert this instruction (accepted by the MIPS assembler): `abs $t2, $t3`. This instruction means that register \$t2 has a copy of register \$t3 if register \$t3 is positive, and the two's complement of register \$t3 if \$t3 is negative. (Hint: it can be done with three instructions.)

6. What is delta delay in VHDL. Please explain how delta delay works with the following example:



Time	Delta	Event
0 ns	1	A: 1->0 eval INVERTER
	2	B: 0->1 eval NAND, AND
	3	C: 1->0 F: 0->1 eval AND
	4	F: 1->0
1 ns		