

COMP3211/9211 11s1

Tutorial 4 (Week 05)

1. Study the example shown in slide P36 of wk3_1, what operation steps can be saved as compared to the multiplication performed by the design shown in slide P31 of wk3_1?
2. Study the shifter design shown in slide P40 of wk3_1. (a) What is the range of the *shift amount* (i.e. the number of bits shifted)? (b) Use an example to demonstrate a 3-bit logic shift operation (c) how to implement an arithmetic shift operation? (d) If the shifter is re-constructed with two levels of 4-to-1 multiplexers, what is the *shift amount* of the new design?
3. [P&H] 4.12.1
4. [P&H] 4.12.3
5. [P&H] 4.12.4
6. [P&H] 4.12.5
7. [P&H] 4.12.6