

COMP3211/9211 11s1

Tutorial 5 (Week 07)

1. For a program of 1000 instructions, how many clock cycles are required to finish the program on a single cycle processor? Can you work out at least how many clock cycles are required on a pipelined datapath? If you can, explain how you came to the result. If you can't, explain why.

2. The table below lists the time of each type of instructions spent in a datapath.

Instruction class	Instruction fetch	Register read	ALU operation	Data access	Register write	Total time
Load word (lw)	200 ps	100 ps	200 ps	200 ps	100 ps	800 ps
Store word (sw)	200 ps	100 ps	200 ps	200 ps		700 ps
R-format (add, sub, and, or, slt)	200 ps	100 ps	200 ps		100 ps	600 ps
Branch (beq)	200 ps	100 ps	200 ps			500 ps

- a. If the datapath is to be pipelined and the pipeline register delay is 10ps, how do you want to partition the datapath?
- b. There could be multiple solutions to the above question (2.a). Please propose a second design and compare this design with the one you obtained for 2.a. Which one is better? Why?
- c. If the time for an ALU operation can be shortened by 25%, will it affect the speedup obtained from pipelining? If yes, by how much? If no, why?
- d. If the ALU operation now takes 25% more time (as compared to the value given in the table), will it affect the speedup? Please give an explanation.

3. Consider executing the following code on the pipelined datapath shown in Figure 1:

```

add    $1,    $2,    $3
add    $4,    $5,    $6
add    $7,    $8,    $9
add    $10,   $11,   $12
add    $13,   $14,   $15
    
```

