

COMP3211/9211 11s1

Tutorial 7 (Week 9)

1. List differences between the DRAM cell design and SRAM cell design.
2. Given SRAM and DRAM, which one do you want to use for the cache in a two-level memory system (i.e. cache and main memory)? Please explain.
3. Why do we need to refresh DRAM? How can DRAM be refreshed?
4. Refer to the three different memory access architectures shown in slide P14 of the wk8_1 lecture notes and determine how many clock cycles are required for fetching four consecutive memory words with each of the architectures. Assume one clock cycle is required for sending an address, 6 clock cycles for accessing memory and one clock cycle for sending data back.
5. The memory hierarchy design is generally effective for reducing the performance gap between the processor and memory? Why? Please give some examples.
6. Elect half of the students in your class for participating in the assessment of other TLB classes in the Week 10 project part 2 presentations.