

COMP3211/9211 11s1

Tutorial 8 (Week 11)

1. Draw the structure of a direct-mapped cache. Use an example to demonstrate how a memory data item is stored in the cache.
2. Explain how to check cache hit/miss in the cache design.

For the following questions 3-5 from the textbook, we assume memory addresses are byte addresses; namely, each address points to a memory location that stores one-byte data.

3. P&H 5.4.1
4. P&H 5.4.2
5. P&H 5.4.3

6. P&H 5.2.2
7. P&H 5.2.3

8. P&H 5.2.4

9. P&H 5.2.5

10. What are the differences between memory direct-mapped cache and multi-way set associative cache?

11. (P&H) 5.3.1
12. (P&H) 5.3.2
13. (P&H) 5.3.3

14. What is a page table? Given a virtual memory space of 64 bit addresses and page size of 2KB, how many entries are there in the page table?

15. What does TLB stand for in virtual memory design? How is it used in memory system? Please draw a diagram to show how a CPU works with a memory system that has cache, main memory and disk three levels.