Overview

- Memory System Hierarchy
- RAM, ROM, EPROM, EEPROM and FLASH

COMP3221/9221: Microprocessors and Embedded Systems

Memory System Hierarchy

- Registers
  - Fastest but most expensive.
- Cache
  - Slower than registers but bigger size.
  - Managed by hardware and therefore typically invisible to programmers.
- On-chip memory (RAM and ROM)
  - An alternative for cache.
  - Managed by the software.
- External memory (RAM and ROM)
  - Slower than on-chip memory but bigger size.
- Auxiliary storage (Hard disk, floppy disk, CDROM)
  - Much slower than external memory but much bigger size.
  - Non-volatile i.e. data exists after the power is switched off.
Computer Types and Memory Maps

- General purpose computer systems
  - Programs and data (including OS) are stored on the auxiliary storage (typically hard disk).
  - A large amount of RAM to store programs and data.
  - When executed, programs are loaded from disk to RAM by OS.
  - ROM to store boot-up code and low-level system I/O drivers.

- Embedded systems
  - Typically no auxiliary storage.
  - Program and constants are stored in ROM or non-volatile memory such as flash.
  - Data are stored in RAM.
    - Program could be copied from ROM to RAM to increase the execution speed.
  - On-chip memory is preferred to cache due to its low power consumption.

Computer Types and Memory Maps (Cont.)

Semiconductor RAM

- Memories are semiconductor integrated circuits.
- A RAM (Random Access Memory) chip consists of an array of memory cells, a decoder for addressing a particular cell, and signals to control the direction of data flow.
An Example Semiconductor RAM

• The CE signal (chip enable, or sometimes CS, chip select) is derived by decoding the rest of address bus.
• R/W controls whether the memory cell is being read from or written to.
• D_i and D_o are separate data-in and data-out pins.
  - Some chips have a single data I/O pin.

Static Memory Cells

• A static memory cell is a flip-flop.
• The transistors could be bipolar or MOS devices.
• The following figure shows a typical static memory cell.

Static Memory Cells

• The bipolar flip-flop works as follows
  - Assume the ROW_SELECT is high (2.5 volts) and that transistor Q1 is on. Current flows through R1 and R2, which are chosen to make the voltage at point A higher than the column line C. Q1' is off, making the voltage at point A' higher than the column line C'. Thus, when the row is not selected, the diodes D1 and D1' isolate the cell from the column lines C and C'. When the cell is read, ROW_SELECT is asserted (it now is 0 volt), point A becomes lower than C, and current flows in diode D1 from column line C. This current could signify a logic one stored in the cell. A logic zero is stored by turning Q1 off and Q1' on. Now, when ROW_SELECT is asserted, the C column line will not have current flow while C' will. Writing into the cell involves asserting the ROW_SELECT and driving either C or C' to set Q1 or Q1' depending on whether zero or one is to be stored.
Dynamic Memory Cells

- A dynamic cell is a capacitor where absence or presence of charge denotes a stored one or zero.
- The following figure shows a typical dynamic memory cell.
  - The MOS capacitor can be written to by activating the row, or word, line to turn the MOS transistor on and charge the capacitor through the column, or bit, line.
  - The cell can be read by turning the transistor on and sensing a voltage on the column.

Static Memory

- Static RAM, or SRAM, consists of array of flip-flops.
- Has lower density and thus lower storage capability than dynamic RAM.
- Simpler to use than dynamic RAM
- Does not need to refreshed like DRAM.

Static Memory (Cont.)

- A problem with dynamic cell is that the charge stored on the capacitor leaks away through the substrate.
  - Thus, the dynamic memory must be refreshed at periodic intervals by activating ROW_SELECT line while holding all column lines at a particular voltage level.
  - All cells in the row can have the capacitor’s charge (or lack of charge) refreshed at once.
Dynamic Memory

The DRAM memory cell requires periodic refresh operation. There are several refresh methods.

- **RAS-only refresh:** This is the most common method of refresh. The row addresses are strobed by asserting RAS while CAS is held high. The cycle must be repeated for every row address.

- **CAS-before-RAS refresh:** CAS-before-RAS eliminates the need for external refresh addresses. If CAS is held low, a specified time before RAS is asserted, on-chip refresh circuitry automatically furnishes the refresh address. This method takes slightly longer time than RAS-only method.

- **Hidden refresh:** This refresh is done while maintaining the latest valid data at the output and extending CAS and cycling RAS.

Pseudostatic RAM

- A memory that combines the high storage capability of DRAM and ease of use of SRAM is pseudostatic RAM.

- It uses DRAM cells and includes on-chip refresh circuitry so that it appears to the user as SRAM.

- Some care must be taken to avoid a conflict when the system attempts to access the memory while an internal refresh is being done. Two approaches may be included in the design of the chip to solve this problem:
  - In the first approach, a separate pin may be included to tell the RAM when it can execute a refresh cycle without conflicting with an external access request. External logic can pulse this input to refresh the chip.
  - In the second approach, a “ready” or “wait” output from the RAM may be used for handshaking in a system where “wait state” can be generated.
ROM Memory

- There are various types of ROM memory chips.
  - Mask programmable ROM are programmed during the manufacturing stage and cannot be programmed by user.
  - Other ROM devices are field programmable and may be programmed by the user. These are called programmable read only memories, and include UV-erasable PROMs (EPROMs), one-time programmable (OTP) EPROMs, and fusible-link PROMs.
    - EPROMs are electrically programmable are erased by irradiating the chip through a quartz window with ultraviolet (UV) light.
    - An OTP EPROM is an EPROM without the window so that once programmed, it cannot be erased.
    - Another type of programmable read only memory is the electrically erasable PROM (EEPROM), which can be programmed and erased while in use.

ROM Memory Cells

- The ROM memory cell is simply a wire or connection made or not made in the programming process.
- The binary information is represented by the presence or absence of the gate on the MOS transistor.
- Activating the word line puts a one or zero on the bit line.

EPROM Memory Cells

- UV Light to Erase
- Quartz Window
- Source
- Drain
- Filed Oxide
- SiO₂
- Si Floating Gate
- p-Substrate
- Electrons injected to program

EPROM Cell
**EPROM Memory Cells (Cont.)**

- The EPROM cell is a MOS transistor without a connection to the gate.
- To program the EPROM, the chip is placed into a PROM programmer and during the programming cycle, the address and data are sent to the chip and the programming voltage is applied. To change the state of the gate, electrons are either injected by an avalanche mechanism into the silicon floating gate or not. This after the programming, the channel between the source and the drain either conducts or does not.
- If the chip needs to be erased, it must be placed into the PROM eraser. The ultraviolet light irradiated from the PROM eraser disperses any charge stored in the floating gate back into the substrate and erases the memory.

**EEPROM Memory Cells**

- The EEPROM is a further development of the EPROM.
- A second polysilicon gate, called the control gate, is added above the floating gate.
- A control voltage may be applied to the gate to program and erase the cell by injecting or disperse electrons in the floating gate.
- EEPROM can be programmed and erased without removing the chip from the circuit in use.
- The time required to write is longer than a comparable RAM chip.
- There is a maximum number of times it can be programmed (the industry standard as of 1993 is 10,000 program/erase cycles).

**FLASH Memory**

- Similar to the EEPROM.
- Its drawback is that the entire memory or page must be erased where single locations can be erased and reprogrammed in the EEPROM devices.
Reading

1. Chapter 9: Computer Memories. Microcontrollers and Microcomputers by Fredrick M. Cady