

COMP 3221

Microprocessors and Embedded Systems

Lectures 32: Memory and Bus Organisation - II

<http://www.cse.unsw.edu.au/~cs3221>

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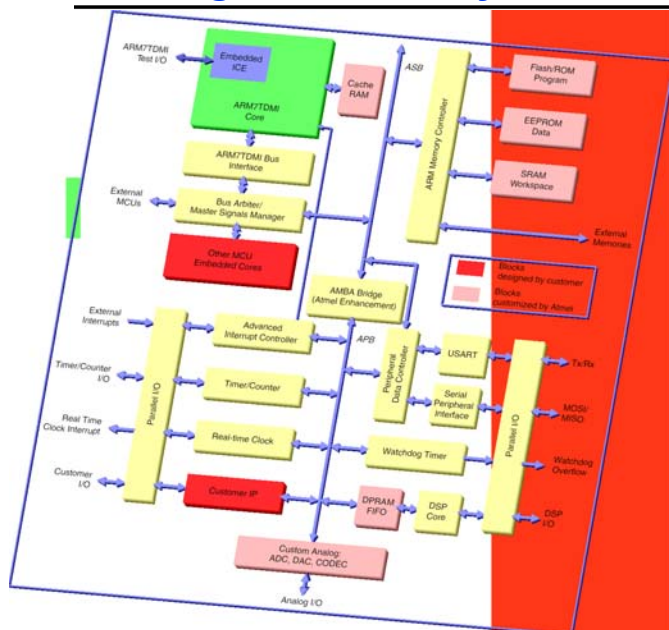
Overview

- ° Bus Hierarchy
- ° ARM's AMBA Bus Standards

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Big Picture: A System on a Chip

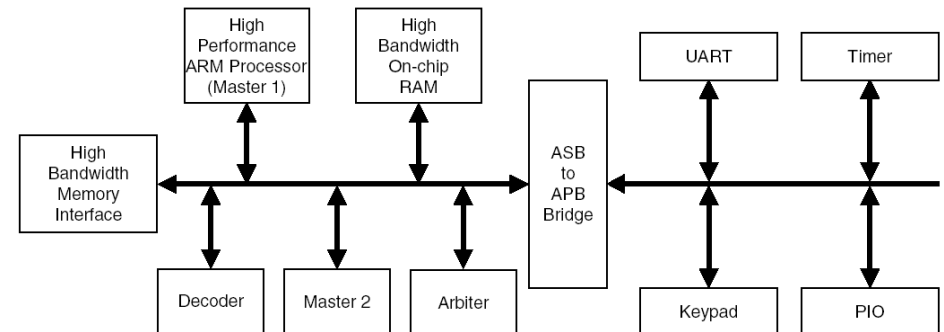


Integration of Core Processor and many sub-system micro-cells

- ARM7TDMI core
- Cache RAM
- Embedded Co-Processors
- External Mem Interface
- Low bandwidth I/O devices
- Timers
- I/O ports

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Review: ARM System Architecture



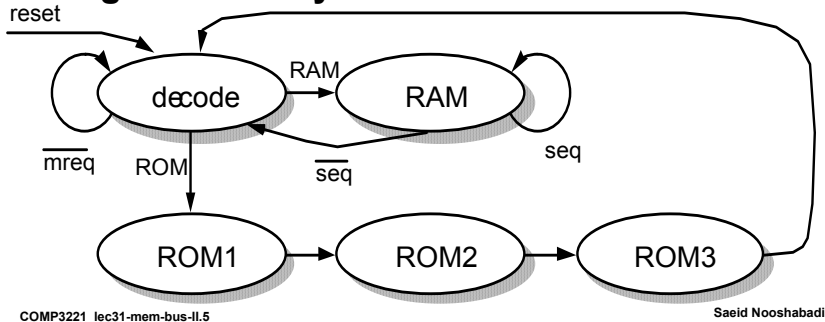
Need a Mechanism to allow various Processing units to access the Memory Bus without causing conflict

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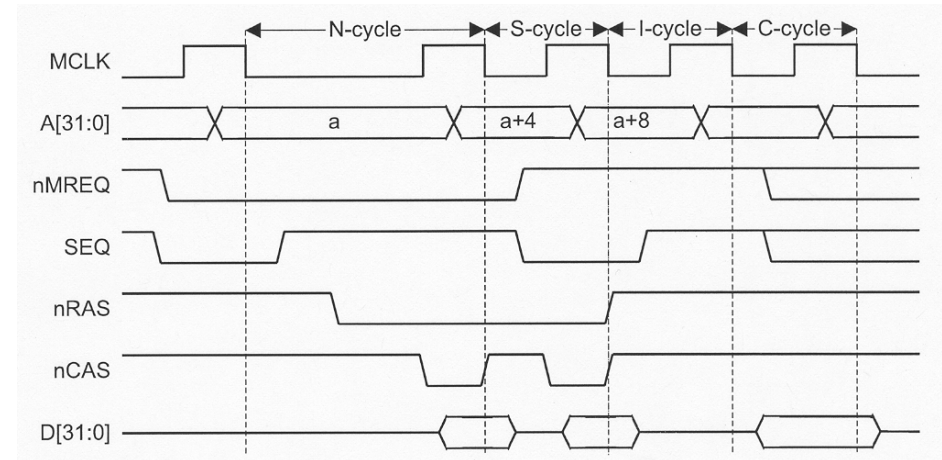
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Review: Memory State Transition Diagram

- ° Processor internal operations cycles do not need access to memory
 - Mem. Access is much slower than internal operations.
 - Use wait states for mem Accesses
 - ° mreq = 1 internal operation
 - ° mreg = 0 memory access
- Internal Operations can run at max speed



Review: Memory Access Timing Summary



° Notice the pipelined memory access

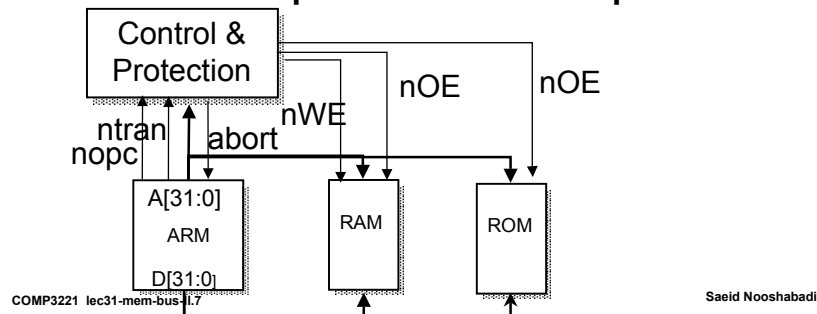
• Address is presented 1/2 cycle earlier

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Support for OS: Memory Protection

- ° Control unit can provide protection to certain areas in user mode:
 - ntran: Processor in USER (=1) or Privileged mode (=0)
 - nopc: memory access is for instruction (=1) or for data (0)
 - abort: caused pre-fetch abort exception



Reading Material

- ° Steve Furber: ARM System On-Chip; 2nd Ed, Addison-Wesley, 2000, ISBN: 0-201-67519-6. [Chapter 8.](#)

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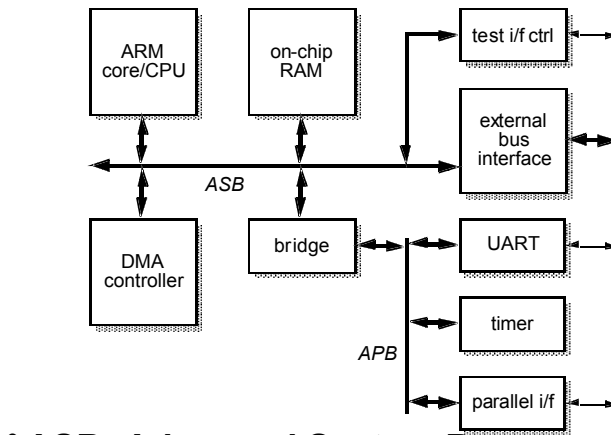
ARM Processor Bus Interface

- Arm Processor is optimised for high speed on-chip cache memory Interfacing
- It is a sub-system embedded in on a larger system
- We need some interfacing rules and protocols to allow interfacing to other sub systems
 - Each sub-systems should follow these rules in order for the system to work properly.
- Options:
 - Making an ad hoc choice in every design
 - Use an established standard
- ARM provides **Advanced Micro controller Bus Architecture (AMBA)**
 - ARM processor uses AMBA to interface to the System Bus

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AMBA Based System



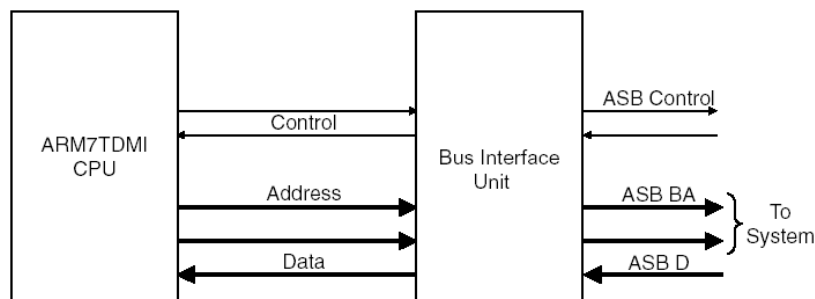
- **ASB: Advanced System Bus: To connect High Performance modules**
- **ABP: Advanced Peripheral Bus: Simpler interface for low performance peripherals**

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ARM Core AMBA Interface

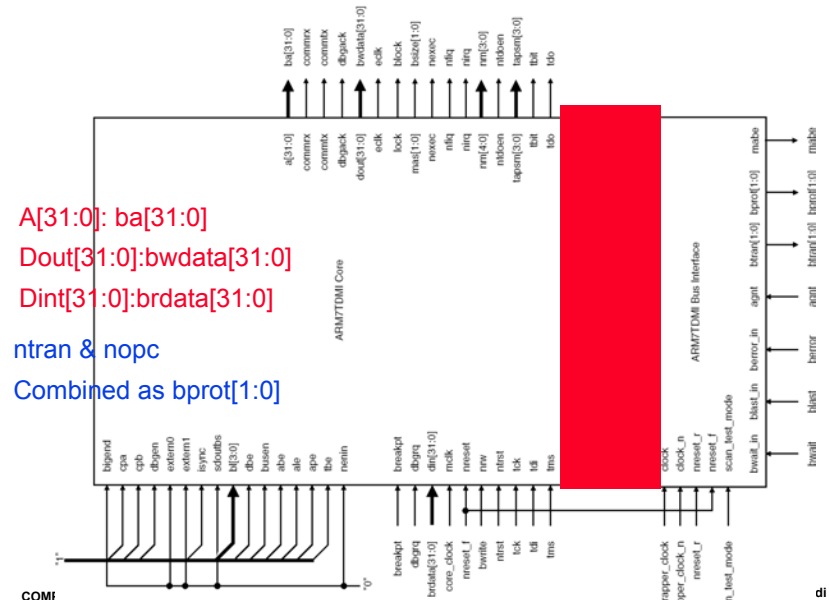
- ARM core cannot understand AMBA signaling standards directly.
 - It needs an interface unit for decoding and translation to AMBA signals
 - Some signals are just renamed



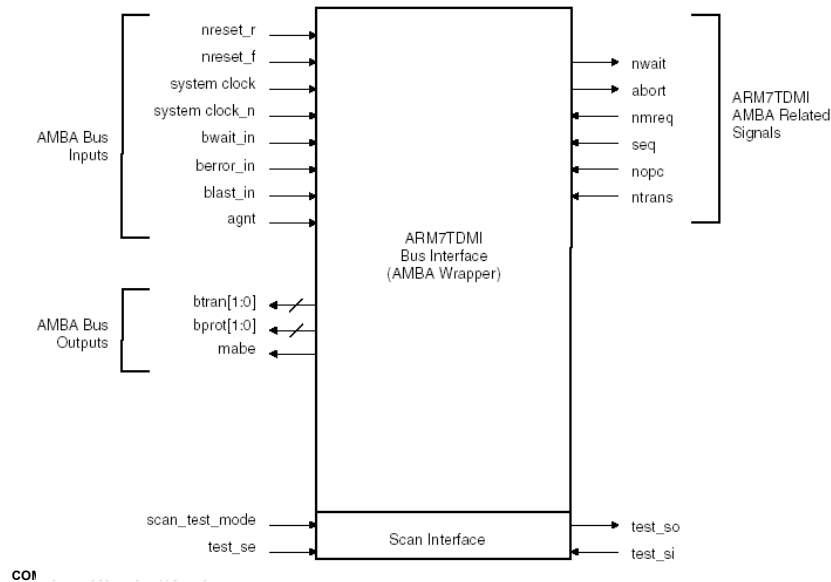
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ARM Core AMBA Interface Details



ARM Core AMBA Interface Wrapper



Important AMBA Features

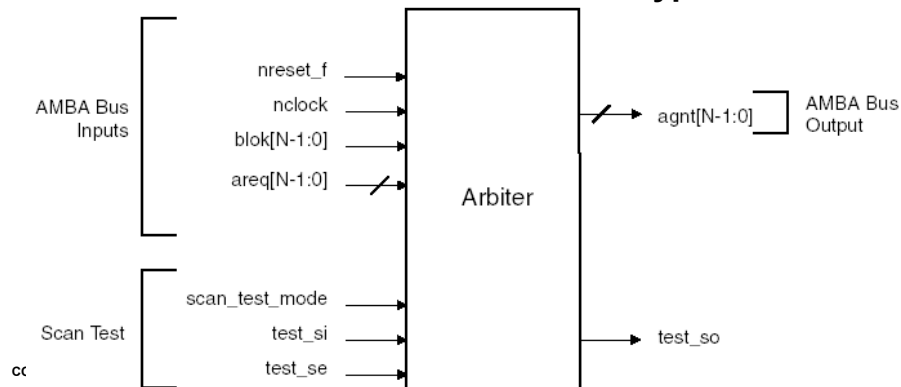
- Allows multiple masters use the Address and Data Bus via some arbitration
 - Only one master can access the bus at any given time
 - Arbitration unit connects to AMBA system Bus
- Allows decoding of addresses issued by multiple masters.
 - Address decoder and Protection unit connect to the AMBA system Bus
- Allows peripheral devices to connect to the system bus via a Bridge

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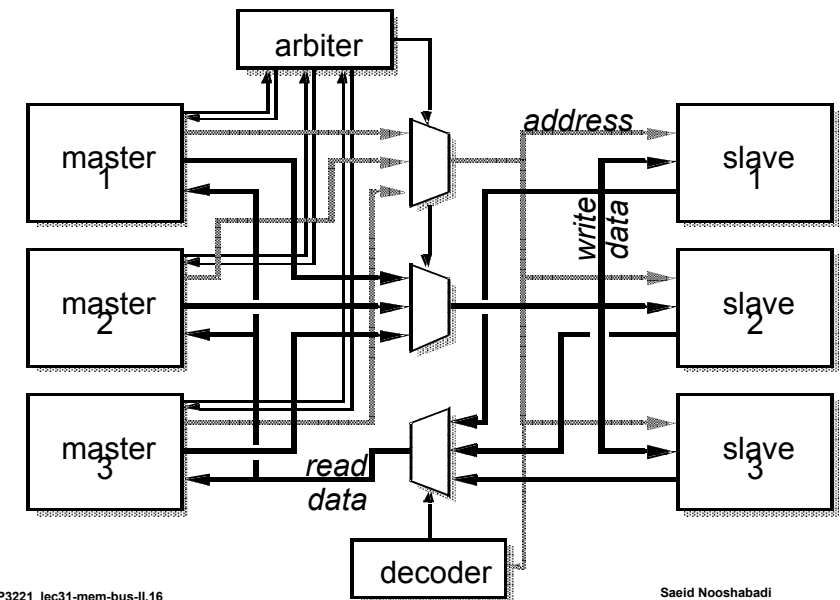
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Arbitration

- Each master x requests for the ASB by issuing $areq[x]$
- When bus is available the arbiter issues a $agnt[x]$ to master x
- Upon receiving $agnt$ signal master issues address and control information to indicate the type of transfer



Simple Arbiter Scheme



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AMBA's ASB Important Signals (#1/4)

- AREQx Bus Request: A signal from bus master "x" to the bus arbiter, which indicates that the bus master requires the bus. There is an AREQx signal for each bus master in the system, as well as an associated bus grant signal, AGNTx.
- AGNTx Bus Grant: A signal from the bus arbiter to a bus master "x", which indicates that the bus master will be granted the bus when BWAIT is low. There is an AGNTx signal for each bus master in the system, as well as an associated bus request signal, AREQx.
- BA[31:0] Address Bus: The system address bus, which is driven by the active bus master.
- BCLK Bus Clock. This clock times all bus transfers. Both the low phase and high phase of BCLK are used to control transfers on the bus.

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AMBA's ASB Important Signals (#2/4)

- BRDATA[31:0] ASB Read Data Bus: This is the system read data bus. The read data bus is driven by the selected bus slave during read transfers.
- BWDATA[31:0] ASB Write Data Bus: This is the system write data bus. The write data bus is driven by the current bus master during write transfers.
- BPROT[1:0] Protection Control: The protection control signals provide additional information about a bus access and are primarily intended for use by a bus decoder when acting as a basic protection unit. The signals indicate if the transfer is an opcode fetch or data access, as well as if the transfer is a supervisor mode access or user mode access. The signals are driven by the active bus master and have the same timing as the address bus.

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AMBA's ASB Important Signals (#3/4)

- BSIZE[1:0] Transfer Size: The transfer size signals indicate the size of the transfer, which may be byte, half-word word. The signals are driven by the active bus master and have the same timing as the address bus.
- BTRAN[1:0] Transfer Type: These signals indicate the type of the next transaction, which may be address-only, nonsequential or sequential. These signals are driven by a bus master when the appropriate AGNTx signal asserted.
- BWAIT Wait Response. This signal is driven by the selected bus slave to indicate if the current transfer may complete. If BWAIT is high, a further bus cycle is required; if BWAIT is low, then the transfer may complete in the current bus cycle. When no slave is selected, this signal is driven by the bus decoder.

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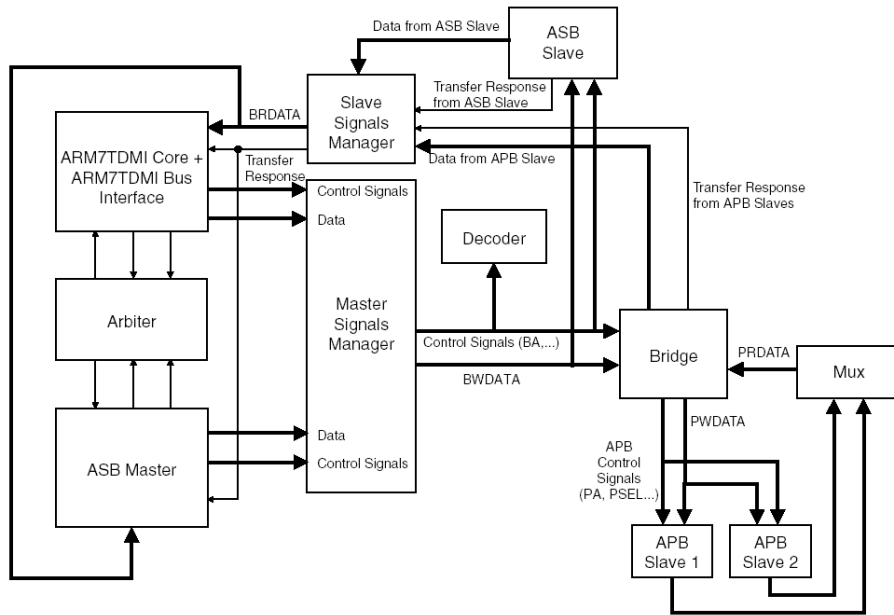
AMBA's ASB Important Signals (#4/4)

- BWRITE Transfer Direction. When high, this signal indicates a write transfer and when low, a read transfer. This signal is driven by the active bus master and has the same timing as the address bus.
- DSELx Slave Select. A signal from the bus decoder to a bus slave "x", which indicates that the slave device selected and a data transfer is required. There is a DSELx signal for each ASB bus slave.
- **SIMILAR SIGNALS for APB**

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ARM SYSTEM Architecture



Summary

- Address decoding is required to select multiple slaves
- Arbitration is required to allow multiple masters access to the bus
- ARM uses AMBA standards for interfacing subsystems
- AMBA has two Buses:
 - ASB: Advanced System Bus
 - APB: Advanced Peripheral Bus