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- Holds recently used data or instructions to save memory accesses.
- Matches slow RAM access time to CPU speed if high *hit rate* (≥ 90 %)
- Is hardware maintained and (mostly) transparent to software
- Sizes range from few kB to several MB.
- Usually a hierarchy of caches (2–5 levels), on- and off-chip.

Good overview in [Sch94].

Cache organisation

- Data transfer unit between registers and cache ≤ 1 word (1–8B)
- Date transfer unit between cache and RAM is *cache line*, typically 16–32 bytes, sometimes 128 bytes and more.
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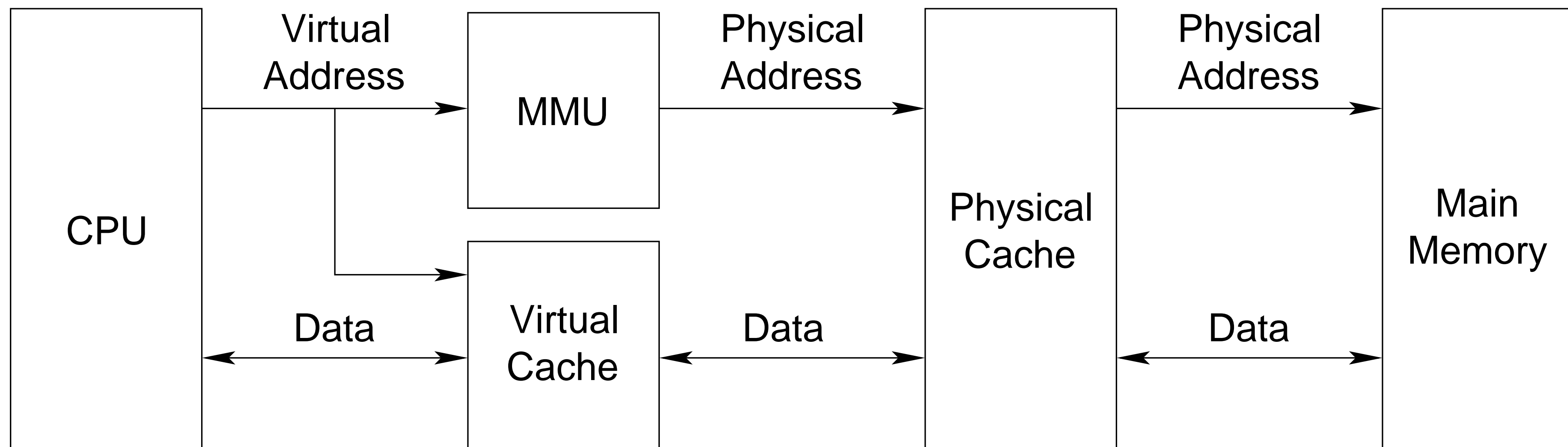
- Each line has associated control info:
  - ➜ valid bit,
  - ➜ modified bit,
  - ➜ tag.
- Cache improves memory access by:
  - ➜ absorbing most reads (increases bandwidth, reduces latency),
  - ➜ making writes asynchronous (hides latency),
  - ➜ clustering reads and writes (hides latency).

Cache access

Virtually indexed: looked up by *virtual address*, operates concurrently with address translation.

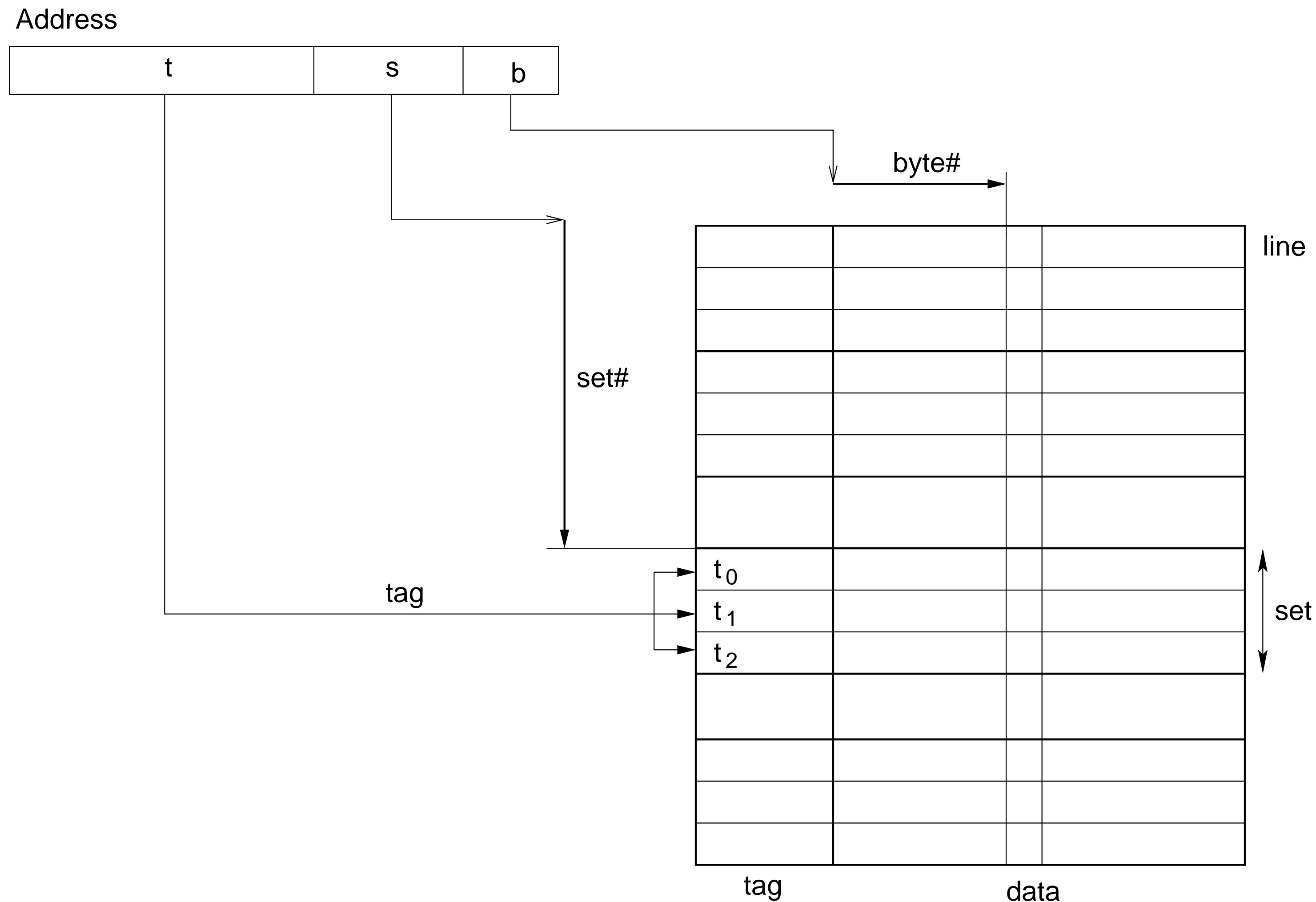
Physically indexed: looked up by *physical address*



CACHE ACCESS MECHANICS

- Address is hashed to produce index of *line set*.
- Associative lookup of line within set
  n lines per set: n*-way set associative cache*.
  - ➜ Typically $n = 1 \ldots 5$.
  - ➜ $n = 1$ is called *direct mapped*.
  - ➜ $n = \infty$ is called *fully associative*, unusual for CPU caches.
- Hashing must be simple (complex hardware is slow)
  $\Rightarrow$ use least-significant bits of address.

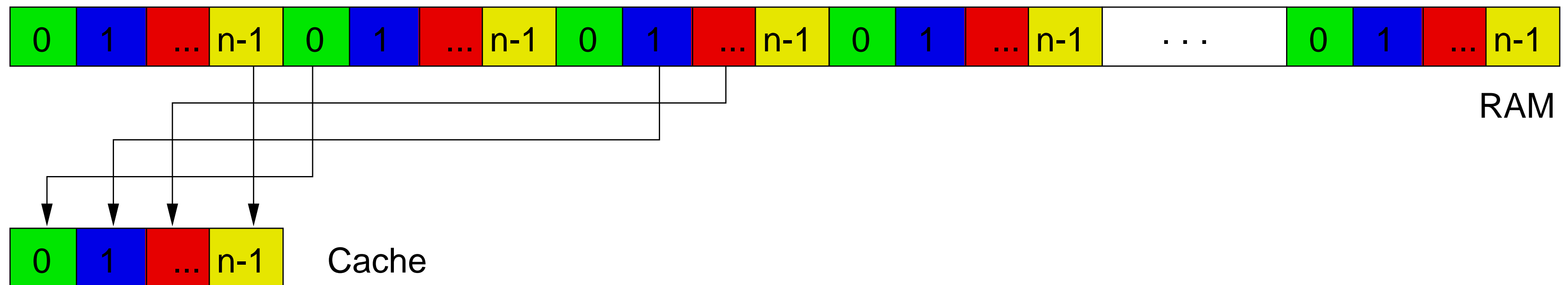
CACHE INDEXING



- ➜ The *tag* is used to distinguish lines of set...
- ➜ ... consists of the address bits not used for indexing.

Cache mapping

- Different memory locations map to same cache line:



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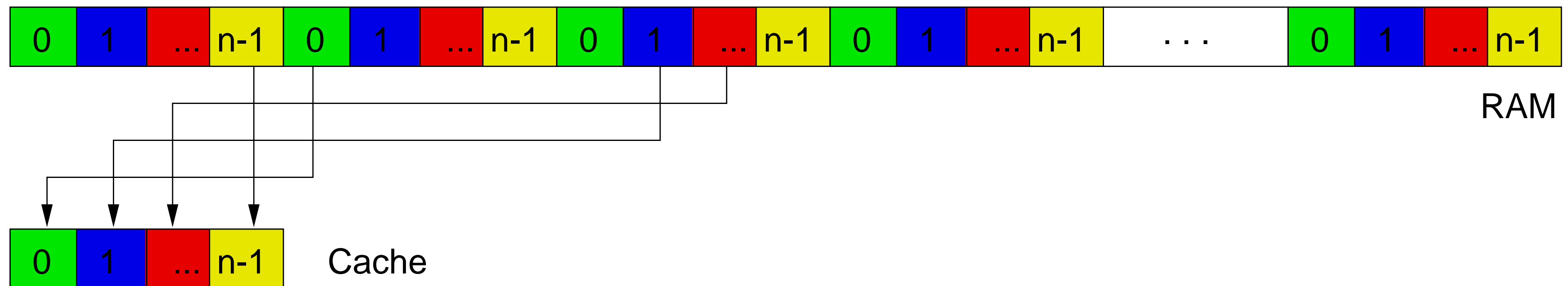

⋆ All memory locations mapping to cache line # i are said to be of *colour* i.

⋆ n-way associative cache can hold n lines of the same colour.
$\Rightarrow$ different types of cache misses:

➜ **capacity misses:** cache is full.

➜ **conflict misses:** set corresponding to address is full, even though there may be unused lines in the cache.

Cache replacement policy

- Indexing (via virtual or physical address) points to line set.
- If all lines of set are valid must replace an existing one.
- Replacement strategy must be simple as it's all done in hardware.
- Dirty bit is used to determine whether a line must be flushed back to memory before invalidation.
- Typical policies:
  - ➜ LRU (or approximation)
  - ➜ FIFO
  - ➜ random

Cache write (update) policy

- Treatment of store operations:
  - **write back:** Stores update cache only,
    memory updated when dirty line is replaced (flushed).
    ➜ Memory is inconsistent with cache.
  - **write through:** Stores update cache **and** memory immediately.
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- Usual combinations: write-back & write-allocate,
  write-through & no-allocate.

Cache types

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- Typically, virtually indexed caches are on-chip, physically indexed caches are off-chip.

Virtual Cache Issues

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- Problem: tag may not uniquely identify cache data!
- Homonyms lead to cache accessing the wrong data!
- Homonym prevention:
  - ➜ *tag* virtual address with *address-space ID* (ASID)
    - ➜ disambiguates virtual addresses (makes them globally valid)
  - ➜ use physical tags
  - ➜ flush cache on context switch
  - ➜ use a SASOS

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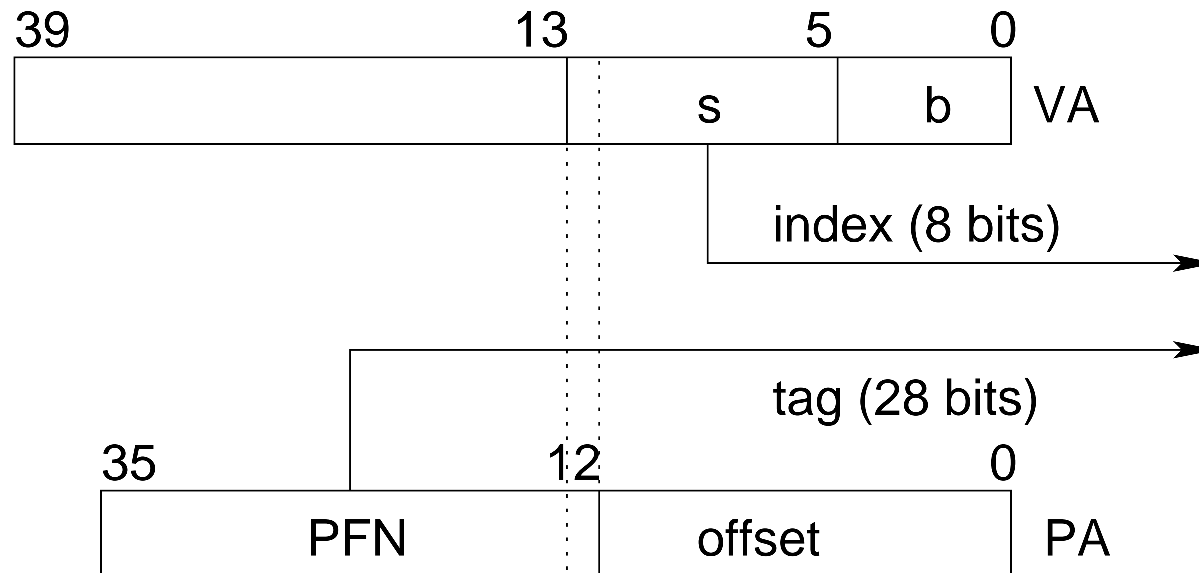
- Physical tagging doesn't help!
- ASIDs don't help either!
- Whether synonyms are a problem depends on cache size and page size!

EXAMPLE: MIPS R4x00 SYNONYMS

- Virtually-indexed, physically tagged on-chip L1 cache
  - ➜ 16kB cache with 32B lines
  - ➜ 4kB (base) page size



- Remember, location of data in cache determined by index
- Tag only confirms whether it's a hit!
- Synonym problem iff $\mathrm{VA}_{12} \neq \mathrm{VA}'_{12}$

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    - ➜ e.g., R4x00: ensure that $VA_{12} = PA_{12}$

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- Doesn't solve synonym problem
- Doesn't solve write-back problem

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- Used on most modern architectures for L1 cache

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- If small or highly associative (all index bits come from page offset) indexing can be in parallel with address translation.
  - ➜ Attractive feature for intermediate level cache.

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⇒ Easy to manage

- If small or highly associative (all index bits come from page offset) indexing can be in parallel with address translation.
  - ➜ Attractive feature for intermediate level cache.
- Cache can use *bus snooping* to receive/supply DMA data
- Usable as off-chip cache with any architecture.

Cache Hierarchy

- Use a hierarchy of caches to balance memory accesses:
  ➜ Small, fast, virtually indexed cache on top (L1 cache).
  ➜ Large, slow, physically indexed cache at bottom (L2–L5).
- Each level reduces and clusters traffic.
- High levels tend to be separated into instruction and data caches.
- Low levels tend to be unified.

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- Some architectures (MIPS, IA-64) use a hierarchy of TLBs:
  - ➜ Top-level TLB is hardware-loaded from lower levels.
  - ➜ Transparent to OS.

TLB Issues

ASSOCIATIVITY

- First TLB (VAX-11/780, [CE85]) was 2-way associative.
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  - ➜ IBM RS/6000 (2-way).
- Superpages $\Rightarrow$ fully associative TLB

SIZE (I-TLB + D-TLB)

Architecture	*TLB Size*
VAX	64–256
ix86	32–32+64
MIPS	96–128
SPARC	64
Alpha	32–128+128
RS/6000	32+128
PA-8000	96+96
Itanium	64+96

Note: not much growth in 20 years!

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- Modern architectures have very low *TLB coverage*.
- Also, many modern architectures have software-loaded TLBs.

$\Rightarrow$ General increase in TLB miss handling cost.

Address Space Usage vs. TLB Coverage

- Each TLB entry maps one virtual page.
- On TLB miss, reloaded from page table (PT), which is in memory.

$\Rightarrow$ Some TLB entries need to map page table.

- ➜ E.g. 32-bit page table entries, 4kb pages.
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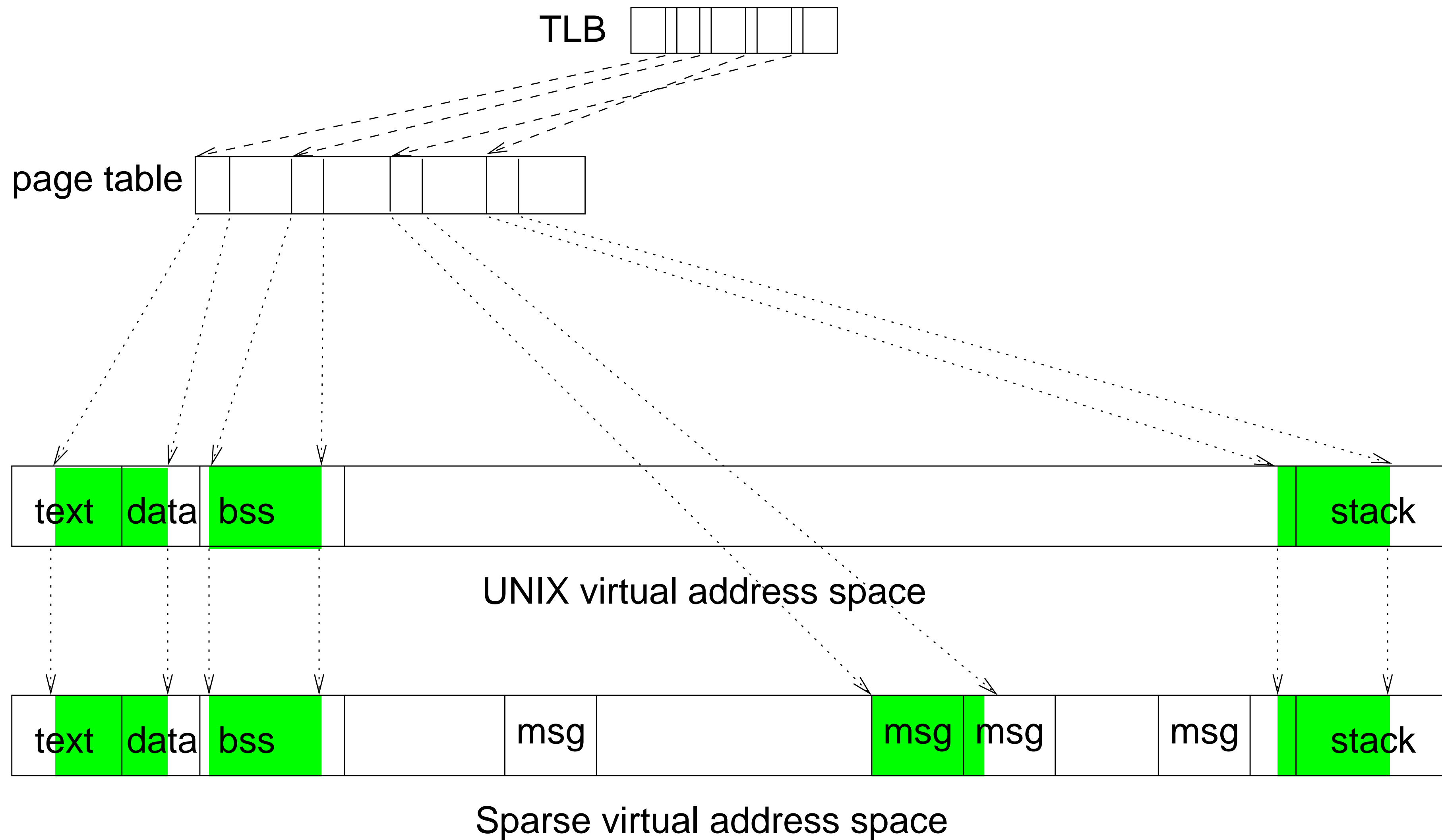
  - ➜ E.g. 32-bit page table entries, 4kb pages.
  - ➜ One PT page maps 4Mb.
- Traditional UNIX process has 2 regions of allocated virtual address space:
  - ➜ low end: text, data, heap,
  - ➜ high end: stack.

  ⇒ 2–3 PT pages are sufficient to map most address spaces.

SPARSE ADDRESS SPACE USE TIES UP PT ENTRIES



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- Modern OS features:
  - ➜ memory-mapped files,
  - ➜ dynamically-linked libraries,
  - ➜ mapping IPC (server-based systems)...
- This problem gets worse 64-bit address spaces:
  - ➜ bigger page tables.
- An in-depth study of such effects can be found in [UNS+94].

References

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[UNS+94] Richard Uhlig, David Nagle, Tim Stanley, Trevor Mudge, Stuart Sechrest, and Richard Brown. Design tradeoffs for software-managed TLBs. *Trans. Comp. Syst.*, pages 175–205, 1994.