Critique of Microkernel Architectures

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Linus Torvalds

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Is Linus right?

MICROKERNEL PERFORMANCE

- First generation μ-kernel systems exhibited poor performance when compared to monolithic UNIX implementations.
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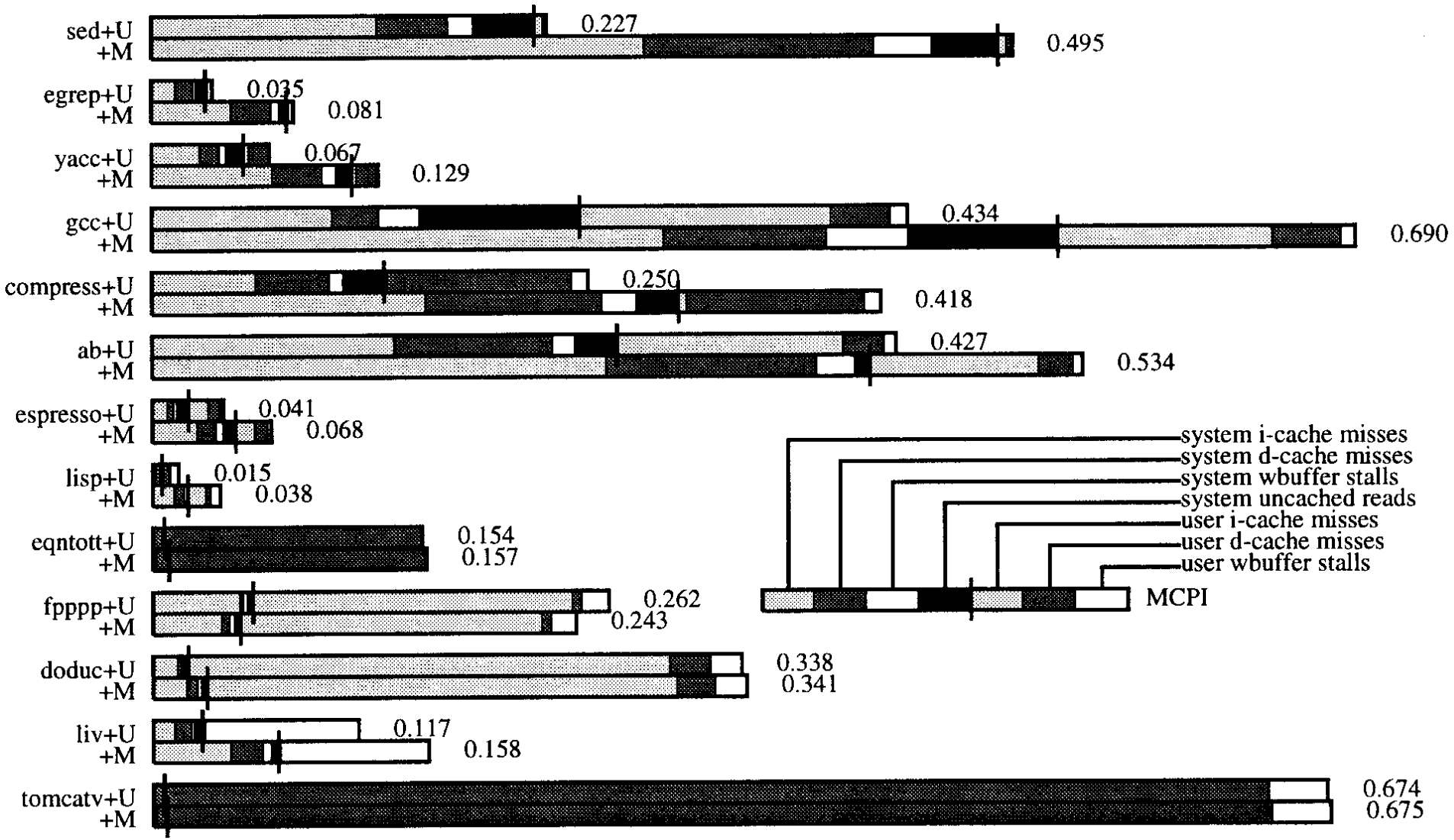
- First generation μ-kernel systems exhibited poor performance when compared to monolithic UNIX implementations.
  - ➜ particularly Mach, the best-known example
- Reasons are investigated by [Chen & Bershad 93]:
  - ➜ instrumented user and system code to collect execution traces
  - ➜ run on DECstation 5000/200 (25MHz R3000)
  - ➜ run under Ultrix and Mach with Unix server
  - ➜ traces fed to memory system simulator
  - ➜ analyse MCPI (memory cycles per instruction)
    - ➜ baseline MCPI (i.e. excluding idle loops)

ULTRIX VS. MACH MCPI



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Claim:

- Degraded performance is (intrinsic?) result of OS structure.
- IPC cost (known to be high in Mach) is not a major factor [Ber92].

ASSERTIONS

1 **OS has less instruction and data locality than user code**.

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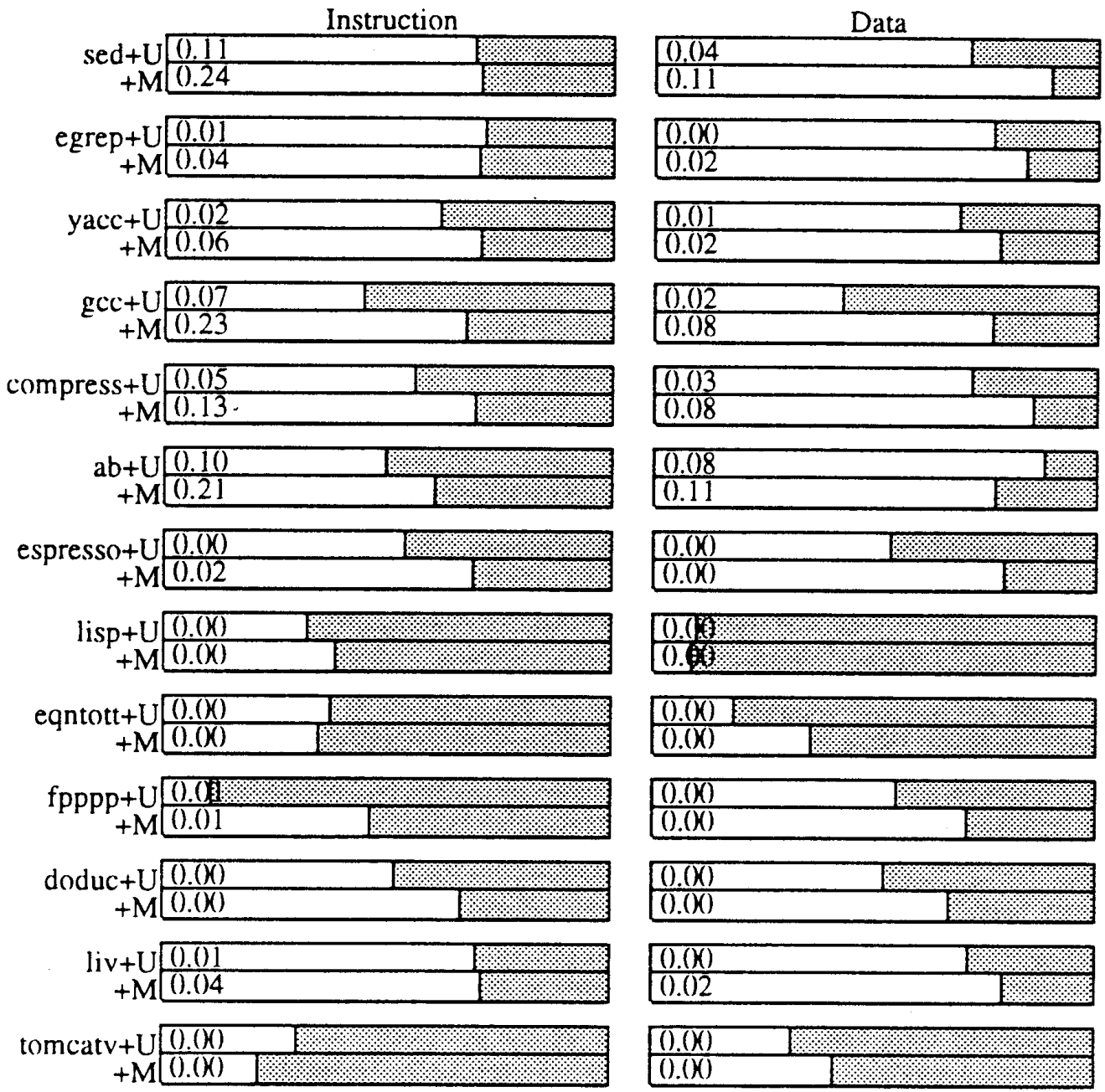
3 **Competition between user and system code is not a problem**
   ➜ Few conflicts between user and system caching.
   ➜ TLB misses are not a relevant factor
   Note: the hardware used has direct-mapped physical caches.
   ⇒ Split system/user caches wouldn't help.

SELF INTERFERENCE



- ➜ Only examine system cache misses.
- ➜ Shaded: System cache misses removed by associativity.
- ➜ MCPI for system-only, using R3000 direct-mapped cache.
- ➜ Reductions due to associativity were obtained by running system on a simulator and using a two-way associative cache of the same size.

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7 **Virtual to physical mapping strategy can have significant impact on cache performance**

- ➜ Unfortunate mapping may increase conflict misses.
- ➜ “Random” mappings (Mach) are to be avoided.

OTHER EXPERIENCE WITH μ-KERNEL PERFORMANCE

- System call costs are (inherently?) high.
  - ➜ Typically hundreds of cycles, 900 for Mach/i486.
- Context (address-space) switching costs are (inherently?) high.
  - ➜ Getting worse (in terms of cycles) with increasing CPU/memory speed ratios [Ous90].
  - ➜ IPC (involving system calls and context switches) is inherently expensive.

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- μ-kernels heavily depend on IPC
- IPC is expensive
  - ⋆ Is the μ-kernel idea flawed?
  - ⋆ Should some code never leave the kernel?
  - ⋆ Do we have to buy flexibility with performance?

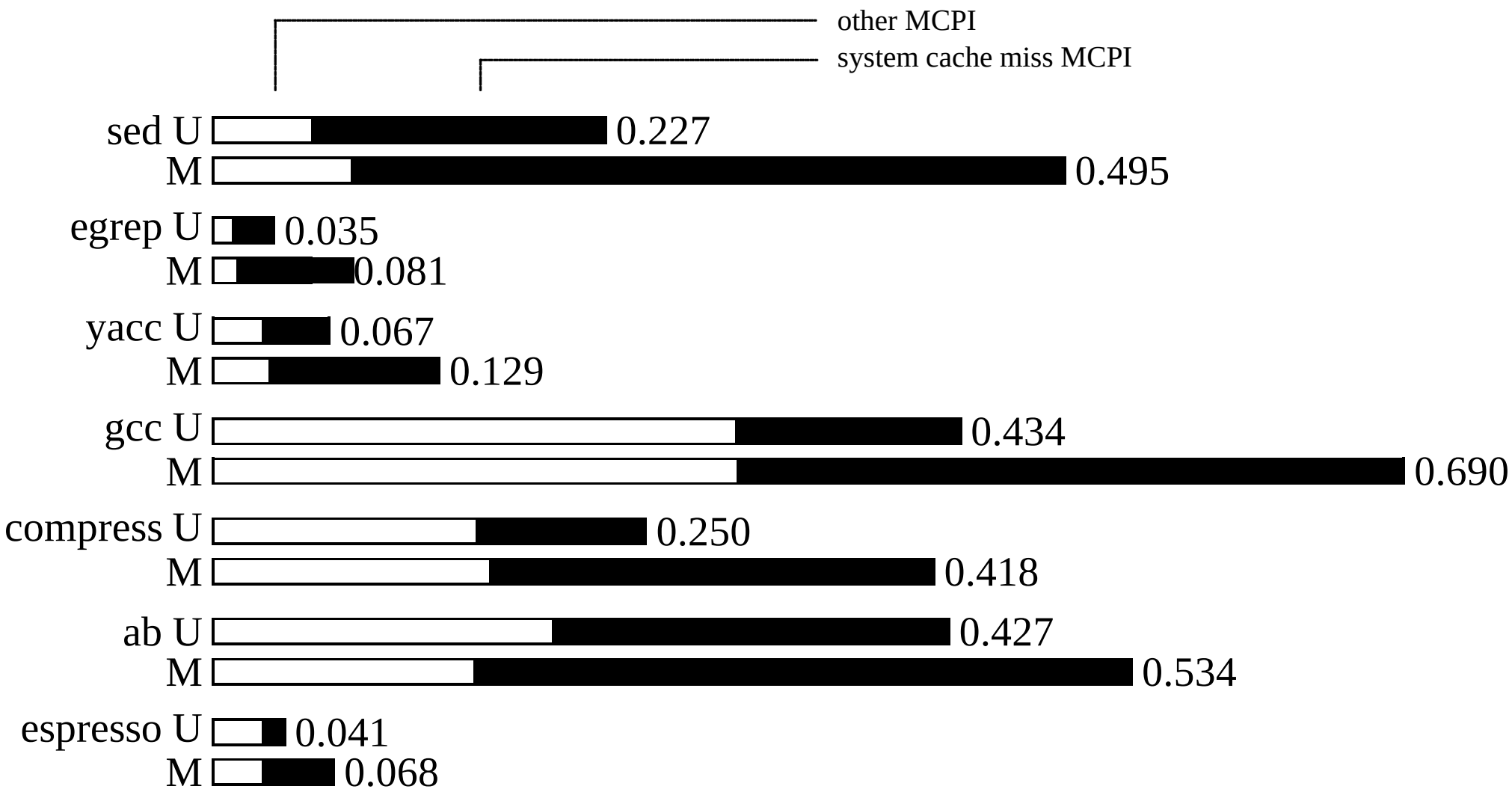
A Critique of the Critique

Data presented earlier:

- ➜ are specific to one (or a few) system,
- ➜ results cannot be generalised without thorough analysis,
- ➜ no such analysis has been done.

$\Rightarrow$ Cannot trust the conclusions [Lie95].

RE-ANALYSIS OF CHEN & BERSHAD'S DATA



MCPI for Ultrix and Mach

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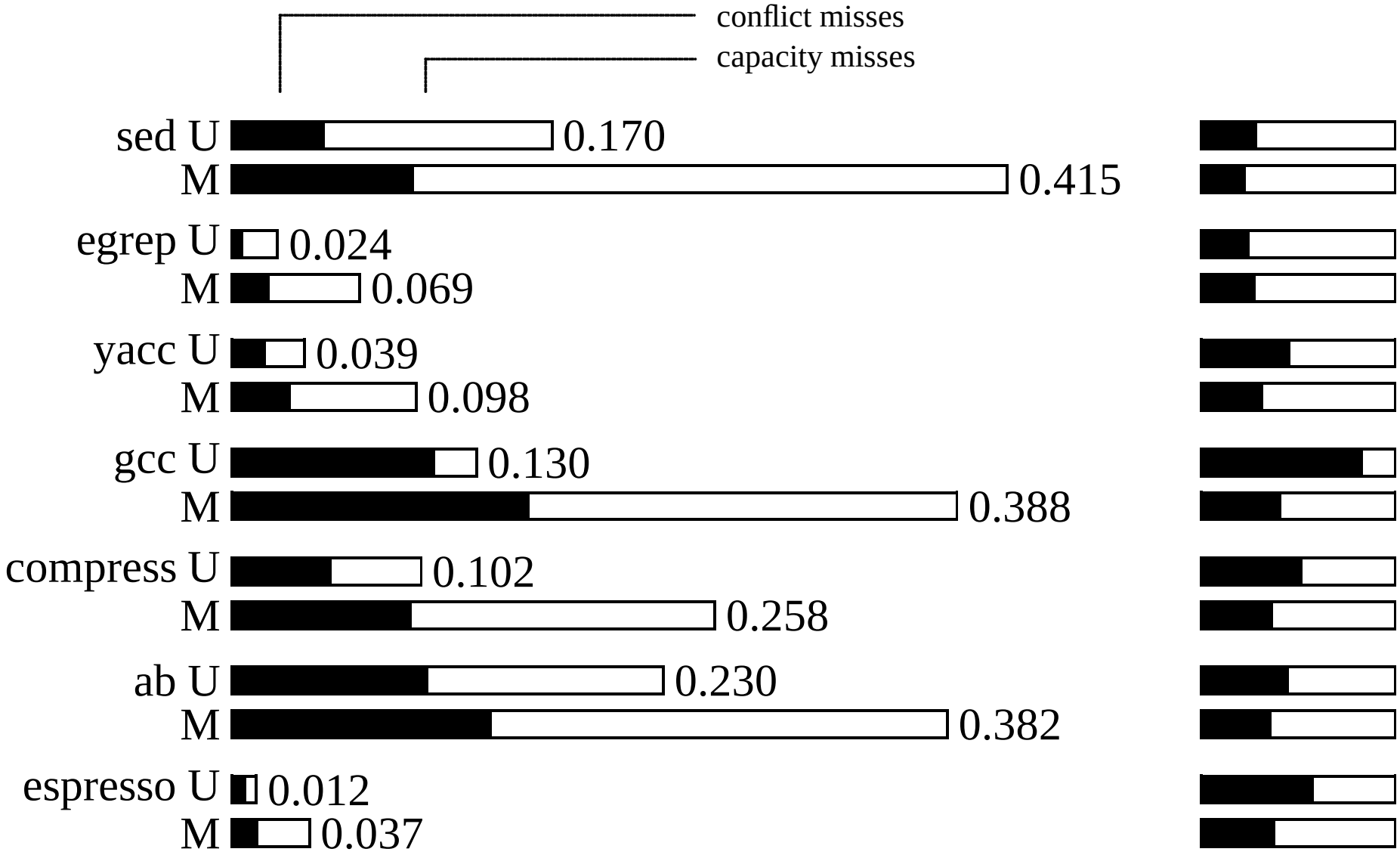

MCPI caused by cache misses: conflict (black) vs capacity (white)

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Can we build μ-kernels which avoid these problems?

REQUIREMENTS FOR μ-KERNELS:

- Fast (system call costs, IPC costs)
- Small (big $\Rightarrow$ slow)

$\Rightarrow$ Must be well designed, providing a minimal set of operations.

Can this be done?

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  - ⋆ L4 kernel call: 123–180 cycles (15–73 cycles overhead).

$\Rightarrow$ Mach's performance is a result of design and implementation **not** the μ-kernel concept!

μ-kernel Design Principles

Minimality: If it doesn't *have to be* in the kernel, it *shouldn't* be in the kernel

Appropriate abstractions which can be made fast **and** allow efficient implementation of services

Well written: It pays to shave a few cycles off TLB refill handler or the IPC path

Unportable: must be targeted to specific hardware

- ➜ no problem if it's small, and higher layers are portable
- ➜ Example: Liedtke reports significant rewrite of memory management when porting from 486 to Pentium

$\Rightarrow$ "abstract hardware layer" is too costly

NON-PORTABILITY EXAMPLE: I486 VS PENTIUM:

- Size and associativity of TLB
- Size and organisation of cache (larger line size - restructured IPC)
- Segment regs in Pentium used to simulate tagged TLB

$\Rightarrow$ different trade-offs

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- Virtual memory/address spaces
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μ-KERNEL DOES *not* HAVE TO PROVIDE:

- file system
  ➜ use user-level server (as in Mach)
- device drivers
  ➜ user-level driver invoked via interrupt (= IPC)
- page-fault handler
  ➜ use user-level pager

L4 IMPLEMENTATION TECHNIQUES

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- Kernel IPC code on single page, critical data on single page
- Many H/W specific optimisations

PERFORMANCE

System	*CPU*	*MHz*	RPC μs	cyc/IPC	semantics
L4	R4600	100	1.7 μs	100	full
L4	Alpha	433	0.2 μs	45	full
L4	Pentium	166	1.5 μs	121	full
L4	486	50	10 μs	250	full
QNX	486	33	76 μs	1254	full
Mach	R2000	16.7	190 μs	1584	full
SCR RPC	CVAX	12.5	464 μs	2900	full
Mach	486	50	230 μs	5750	full
Amoeba	68020	15	800 μs	6000	full
Spin	Alpha 21064	133	102 μs	6783	full
Mach	Alpha 21064	133	104 μs	6916	full
Exo-tlrpc	R2000	116.7	6 μs	53	restricted
Spring	SparcV8	40	11 μs	220	restricted
DP-Mach	486	66	16 μs	528	restricted
LRPC	CVAX	12.5	157 μs	981	restricted

Case in Point: L^4Linux [Härtig *et al*. 97]

- Port of Linux kernel to L4 (like Mach Unix server)
  - ➜ single-threaded (for simplicity, **not** performance)
  - ➜ is pager of all Linux user processes
  - ➜ maps emulation library and signal-handling code into AS
  - ➜ server AS maps physical memory (& Linux runs within)
  - ➜ copying between user and server done on physical memory
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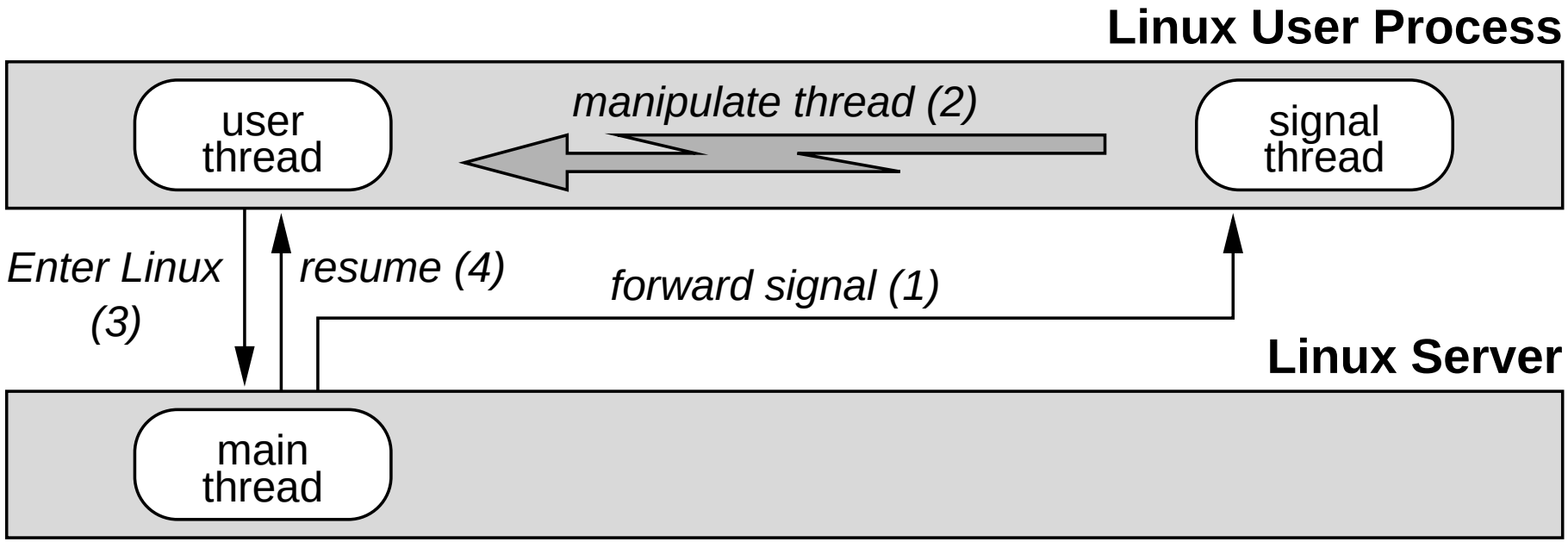
    - ➜ use software lookup of page tables for address translation
- Changes to Linux restricted to architecture-dependent part
- Duplication of page tables (L4 and Linux server)
- Binary compatible to native Linux via trampoline mechanism
  - ➜ but also modified `libc` with RPC stubs

SIGNAL DELIVERY IN L^{4}LINUX



- separate signal-handler thread in each user process
  - ➜ server IPCs signal-handler thread
  - ➜ handler thread ex_regs main user thread to save state
  - ➜ user thread IPCs Linux server
  - ➜ server does signal processing
  - ➜ server IPCs user thread to resume

L^4Linux Performance

MICROBENCHMARKS:

System	*Time [μs]*	*Cycles*
Linux	1.68	223

`getpid()` on 133MHz Pentium

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MkLinux in-kernel	15.66	2050
MkLinux server	110.60	14710

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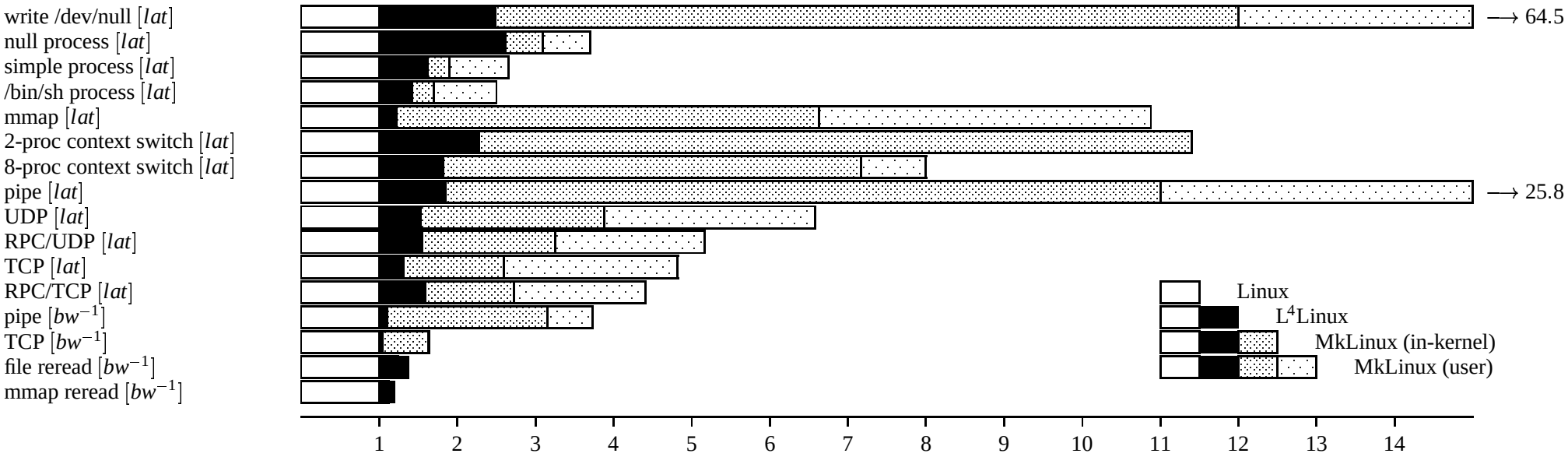
CYCLE BREAKDOWN:

Client	*Cycles*	*Server*
enter emulation lib	20	
send syscall message	168	wait for msg
	131	Linux kernel
receive reply	188	send reply
leave emulation lib	19	

Hardware cost: 82 cycles

MACROBENCHMARKS: LMBENCH



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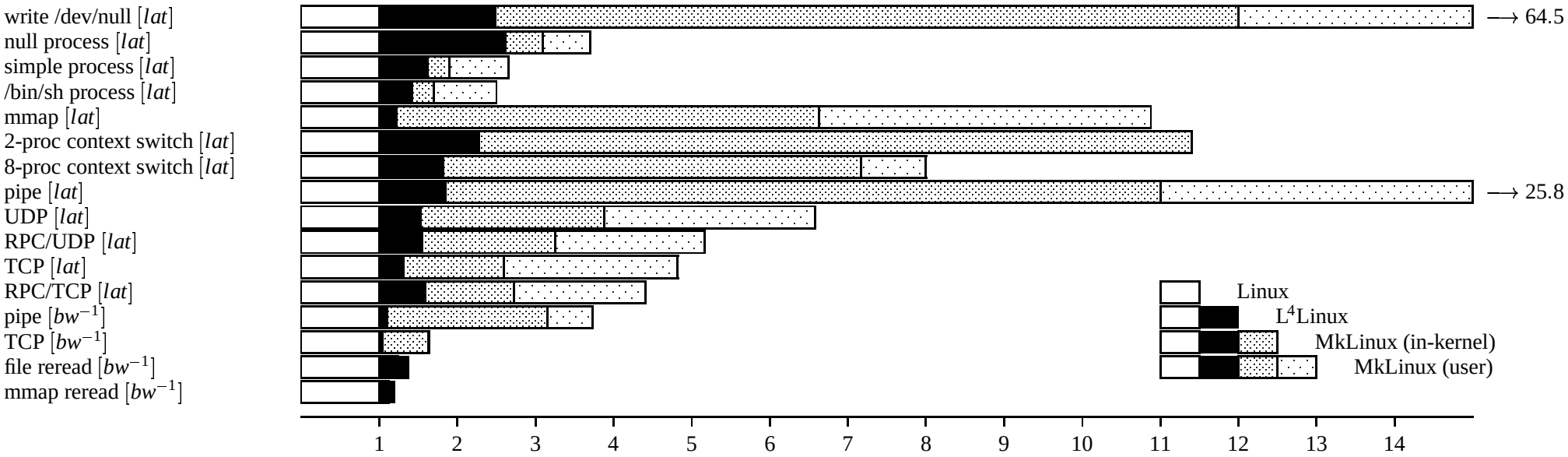
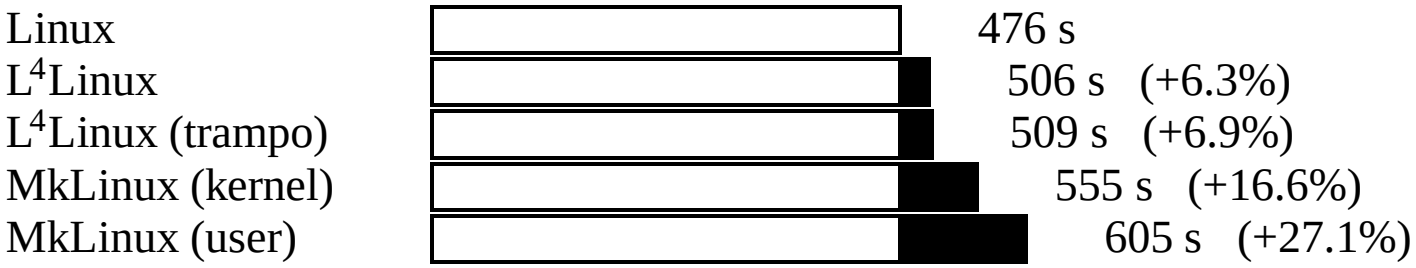


MACROBENCHMARKS: KERNEL COMPILE



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- L4 shows that performance *might* be deliverable
  - ➜ L^4Linux gets close to monolithic kernel performance
  - ➜ need real multi-server system to evaluate μ-kernel potential
- Jury is still out!
- Mach has prejudiced community (see Linus...)
  - ➜ It'll be an uphill battle!

References

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