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Features:

- segregated capabilities,
- single-level store,
- persistence (via checkpointing),
- fast,
- mandatory access control,
- formal proof of confinement [SW00].

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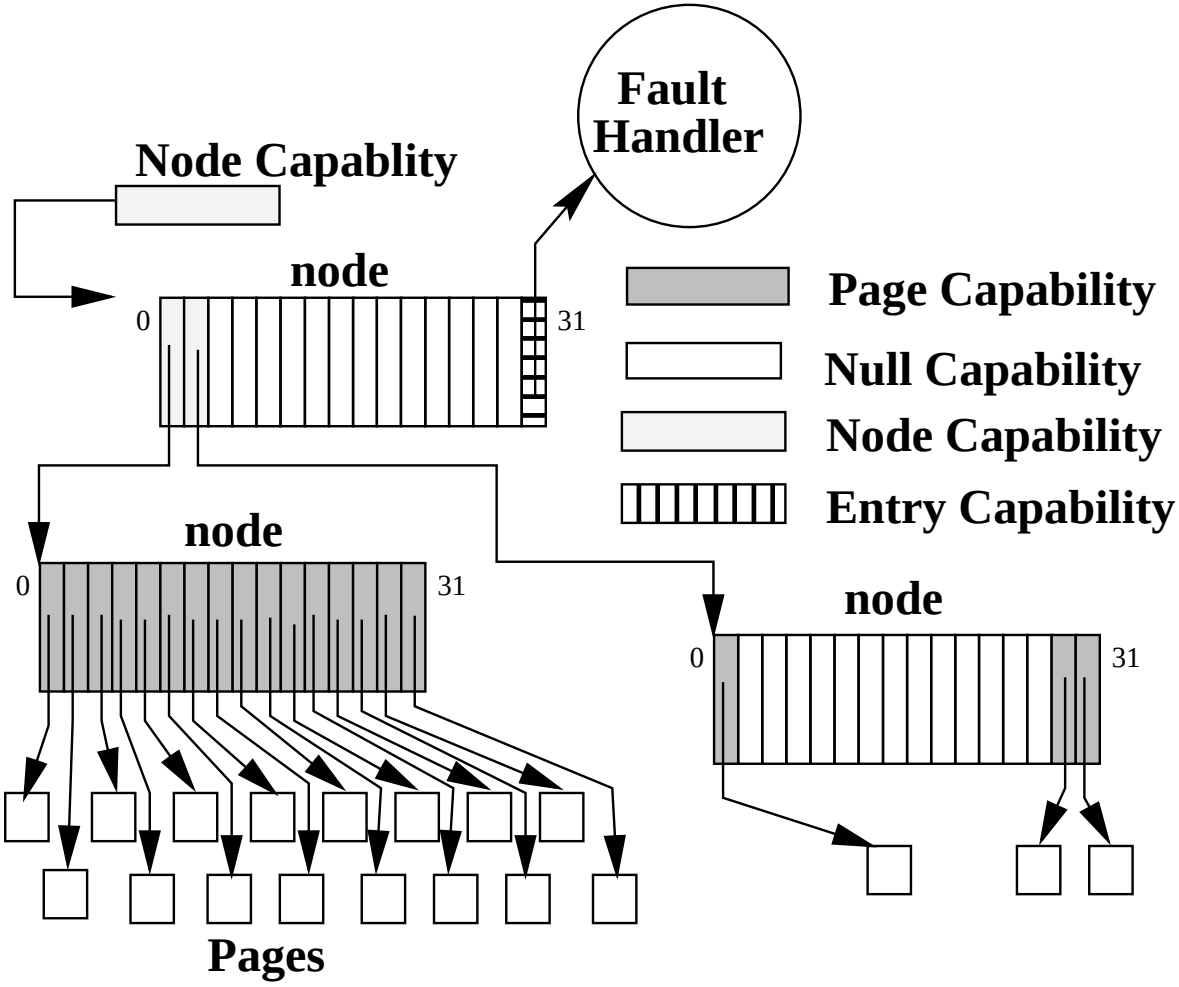
EROS is a re-design of KeyKOS [BFF+92].

EROS MEMORY AND ACCESS MANAGEMENT



Clists form page table

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    - ➜ can obtain *transitive read-only access*
  - ⋆ indirection:
    - ➜ *Reference monitor* (similar to L4 *chief* mediates cap transfer
    - ➜ inserts *forwarding objects* to capabilities
    - ➜ implements security policy
    - ➜ on change of policy can revoke caps by revoking forwarding object

EROS PERFORMANCE

Benchmark	*Linux-Normalized*	*Speedup*
Pipe Latency	5.66 μs / 8.34 μs	32.3%
Pipe Bandwidth	281 MB/s / 260 MB/s	8.07%
Create Process	0.664 ms / 1.92 ms	65.3%
Ctxt Switch	1.19 μs / 1.26 μs	5.5%
Grow Heap	20.42 μs / 31.74 μs	35.7%
Page Fault	3.67 μs / 687 μs	99.5%
Trivial Syscall	1.6 μs / 0.7 μs	-128%

Note: No data on cost of indirection for MAC.

Cool Stuff: Soft Timers [AD99]

PROBLEM: WANT HIGH-RESOLUTION TIMERS

E.g.: Timeouts in L4, prefer high resolution.

- ➜ Kernel has wakeup queues
- ➜ Kernel sets timer interrupt at certain frequency.
- ➜ At each interrupt (tick) checks wakeup queue.

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- ➜ Kernel has wakeup queues
- ➜ Kernel sets timer interrupt at certain frequency.
- ➜ At each interrupt (tick) checks wakeup queue.
- ➜ Handling interrupts is costly.
- ➜ Handling interrupt pollutes cache.
- ➜ Cannot have very high frequency timer ticks.

What can we do?

IDEA: SOFT TIMERS RATHER THAN HARDWARE INTERRUPT

- Check wakeup queues when cost of handling with them is low.
- This is generally the case when in the kernel already.
- Do it at a time where minimal state needs to be saved.

IDEA: SOFT TIMERS RATHER THAN HARDWARE INTERRUPT

- Check wakeup queues when cost of handling with them is low.
- This is generally the case when in the kernel already.
- Do it at a time where minimal state needs to be saved.
- Suitable times:
  - ➜ just before returning from system call,
  - ➜ at the end of exception handling,
  - ➜ at the end of interrupt handling,
  - ➜ in idle loop.

LIMITATIONS OF SOFT TIMERS:

- No absolute, only *probabilistic* accuracy.
- Actual accuracy depends on frequency of trigger events.
- Can enforce absolute upper bound on delay via timer tick.

The Return of the Dumb Terminal: SLIM [SLN99]

PROBLEM: HIGH COST-OF-OWNERSHIP OF PCS

- PCs are expensive to maintain/administrate as individual machines.
- Would be cool to have the power of a big iron occasionally.
  - ➜ There's still (or again?) some attraction in big central servers.

IDEA: STATELESS THIN-CLIENT ARCHITECTURE

- ➜ Stateless (other than frame buffer) cheap terminals (graphic displays),
- ➜ server sends 2D bitmaps,
- ➜ connected via 100Mbps ethernet.

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Supported by very simple, low-level display protocol (5 commands):

① SET: set pixes in rectangle to literal value

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Benchmarked GUI apps: photoshop, netscape, framemaker, MPEG, quake

How to Roll Your Own Tagged TLB and Caches

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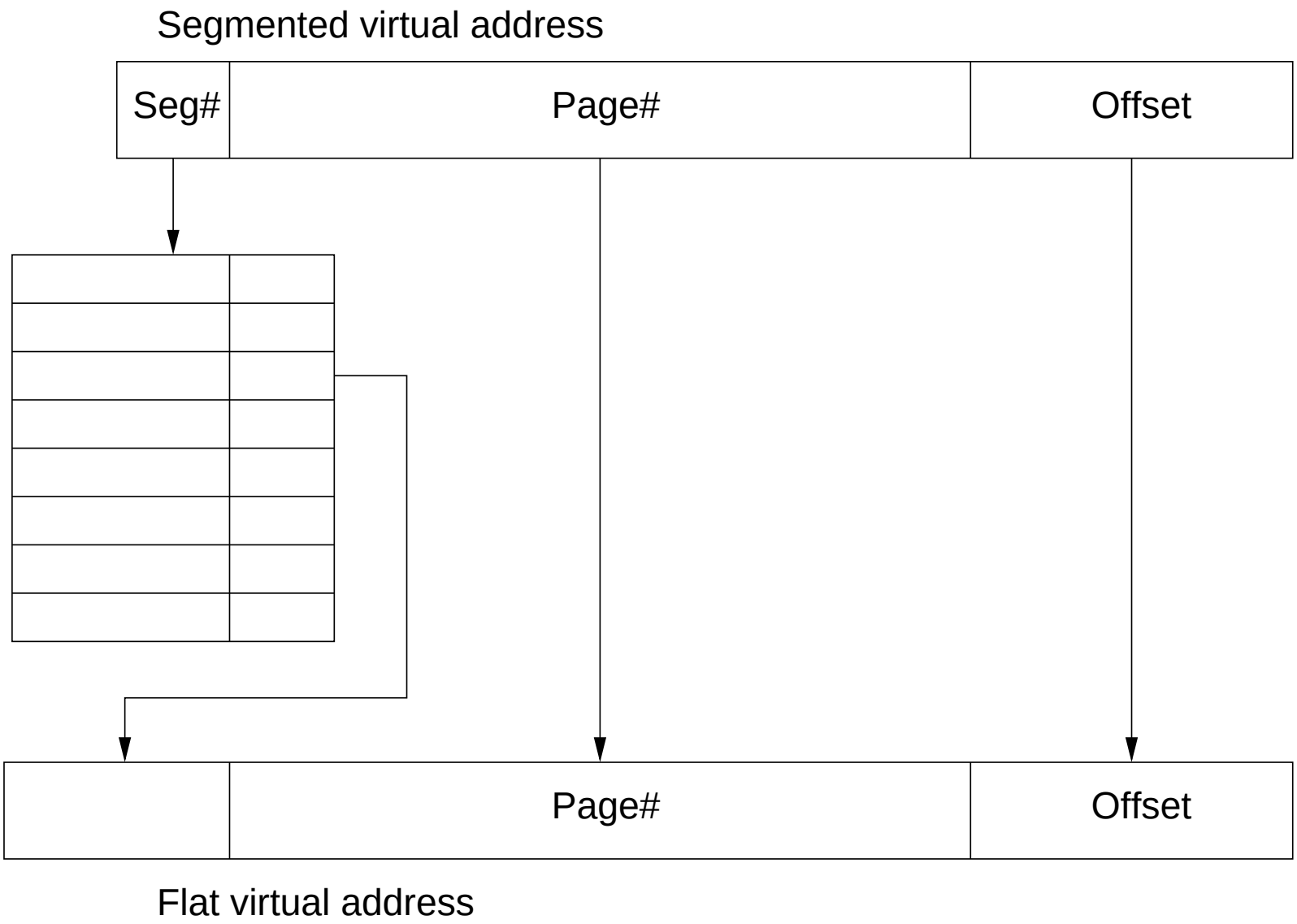
CONTEXT SWITCH WITH UNTAGGED TLB:

- ➜ load *translation table base register* to replace page table
- ➜ flush instruction TLB
- ➜ flush data TLB
- ➜ flush instruction cache (if virtual)
- ➜ flush data cache (if virtual)

⇒ High overhead

SIMULATING TLB TAGS BY SEGMENTATION:



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- Fill all segment registers with process' ASID
- Problem if flat VAS is only 32-bit (Pentium)
- Partial solution [Lie95]:
  - ➜ split AS into *large* (3GB) and *small* area
  - ➜ small area split into smaller (128MB) *slots*
  - ➜ put small processes into a slot
  - ➜ can do fast context switches between one large and all small processes

ON NON-SEGMENTED ARCHITECTURE (STRONGARM)

- StrongARM SA-1100 is a high-performance low-power processor
- Designed for embedded applications
- Some less attractive features (for multitasking):
  - ➜ virtually indexed, virtually tagged caches,
  - ➜ untagged, hardware-loaded TLB.

ARM PAGE TABLES

- Top-level PT entry can:

  ➜ map a 1MB *section*;
  protection with section granularity,
  ➜ point to a second-level PT.

- Second-level PT entry can:

  ➜ map a 64kB *large* page,
  ➜ map a 4kb *small* page.

  Protection with 1/4 page granularity.

- Each page or section is tagged with a *domain id*

ARM DOMAINS

Additional access-control feature:

- 16 different domains,
- domain access control register (DACR) defines accessibility for each:
  - no access
  - access according to page permission bits
  - access irrespective of page permission bits

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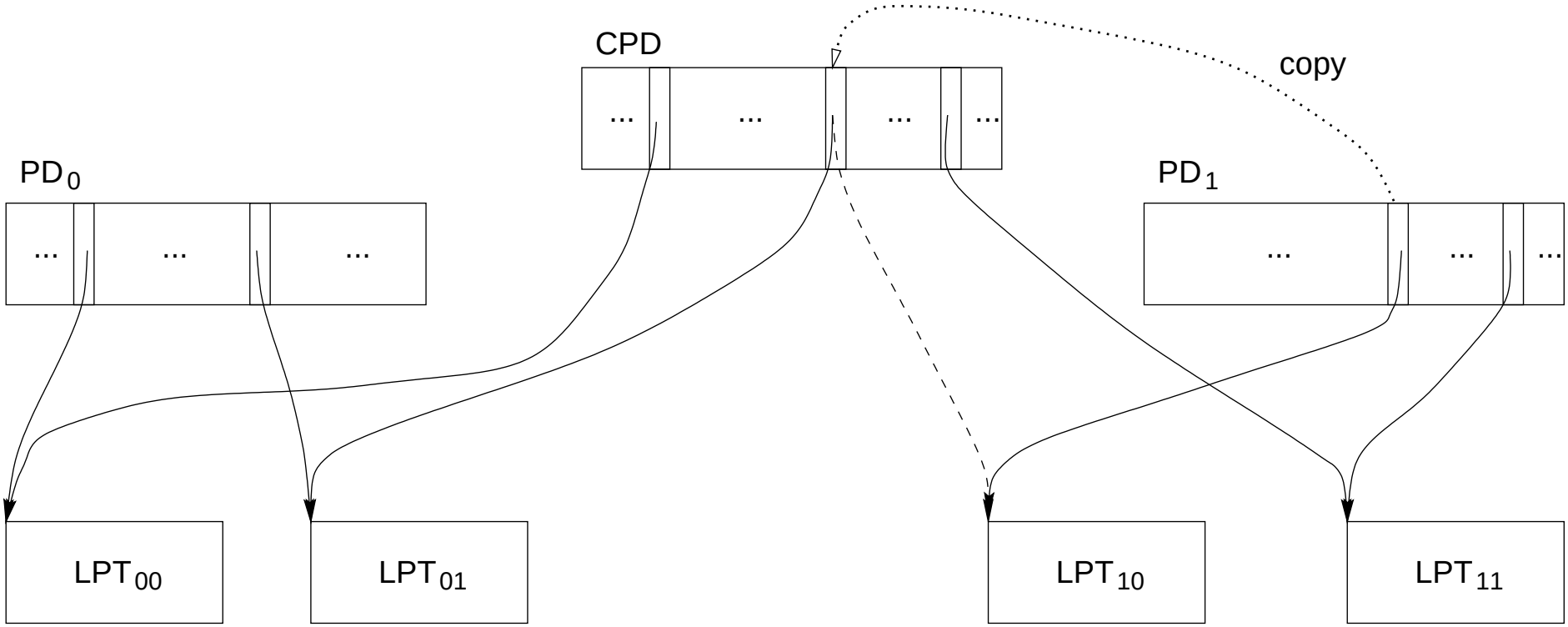
HOW TO AVOID FLUSHING?

- Can avoid flushes if *no overlap of address spaces*
- How????
- Two-part approach [WH00]:
  - ➜ delay flushes as long as possible
    in microkernel
  - ➜ avoid overlaps as much as possible
    in server

DELAYING FLUSHES: IDEA

- Don't change hardware page tables.
- Have translation table base register point to a *cache of top-level page table entries* (CPD).
- Use domain IDs as address-space tag.
- Flush TLB entries and caches when replacing CPD entry.

CACHING PAGE DIRECTORY



CONTEXT SWITCH:

- Set software PT pointer to reference new context's page table
- Load DACR to:
  - ➜ "access according to page permission bits" for new context's domain,
  - ➜ "no access" for other domains
- Go!

No flushes required as long as have separate domain per context.

CACHE REPLACEMENT

- Domains ensure that CPD entries belonging to wrong context raise *domain fault* exception.

- Handled by:

  ➜ replacing CPD entry
  ➜ flushing TLBs and caches

  ⇒ flush only in case of actual collision.

- Also need to flush if recycling domains.

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- Server to allocate process data & stack at unique addresses
  $\Rightarrow$ mini-SASOS (single-address-space OS)
- Need to use separate domains for shared (text). segments
- Aliasing still a problem.

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