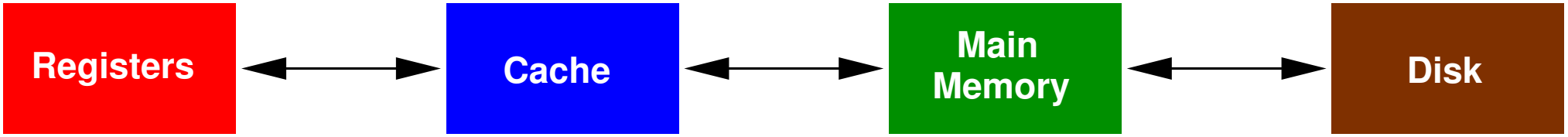
Caching

From an OS Perspective

COMP9242 2005/S2 Week 3

CACHING



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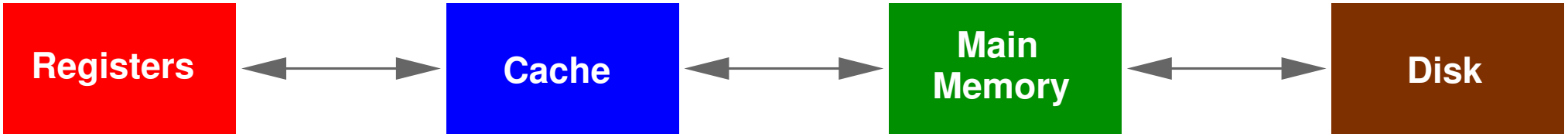

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- Holds recently used data or instructions to save memory accesses.
- Matches slow RAM access time to CPU speed if high *hit rate* ($\geq 90\,\%$)
- Is hardware maintained and (mostly) transparent to software
- Sizes range from few kB to several MB.
- Usually a hierarchy of caches (2–5 levels), on- and off-chip.

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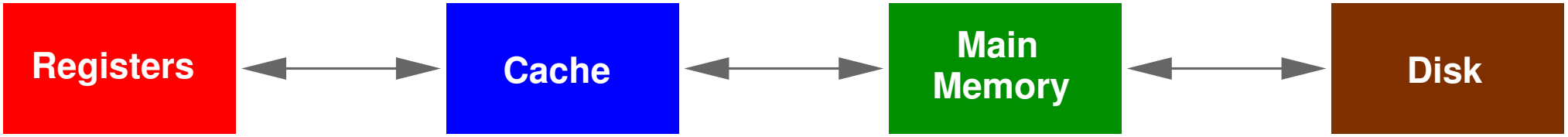

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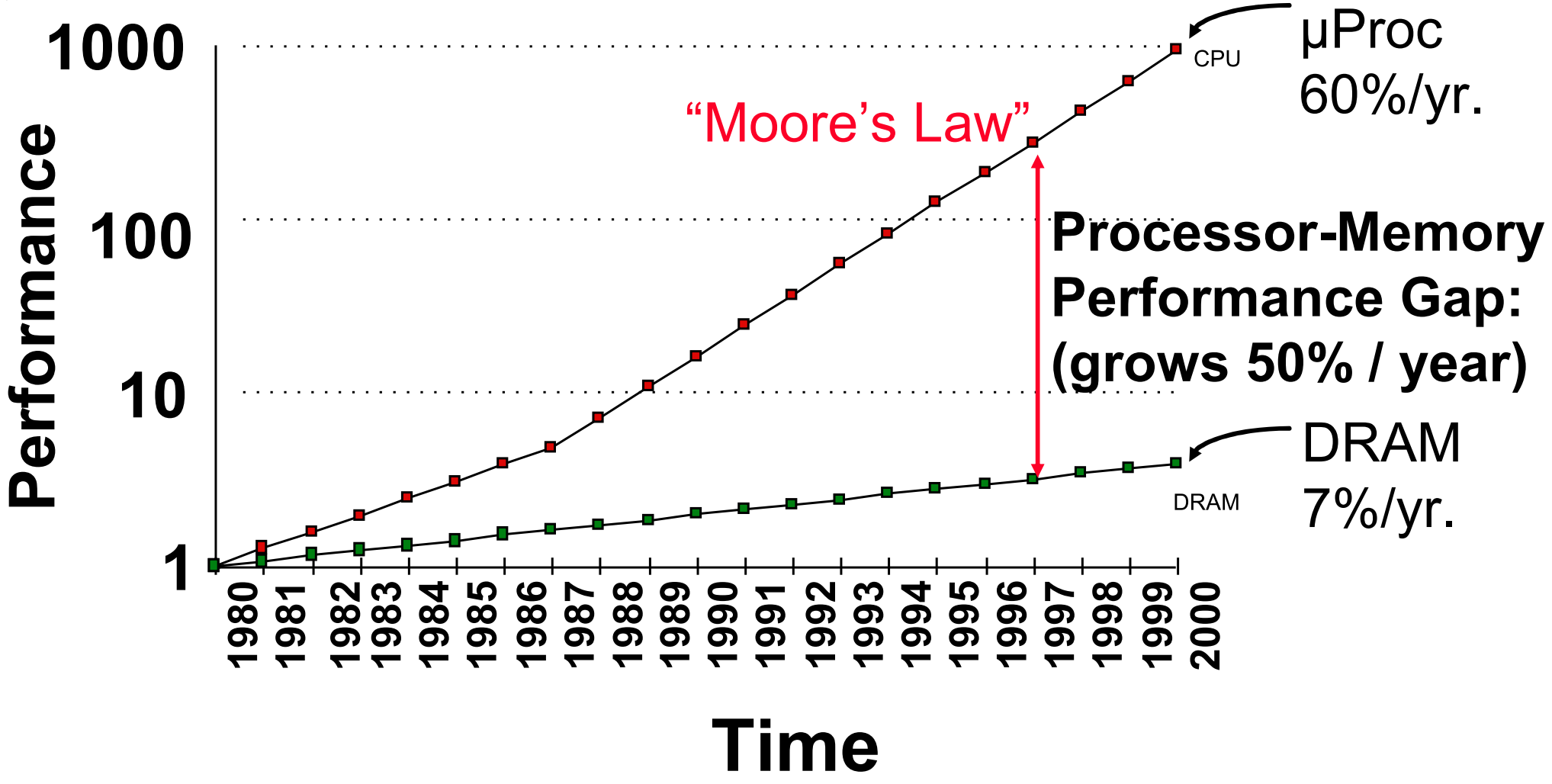
Good overview in [Sch94].

THE MEMORY WALL



CACHE ORGANISATION

- Data transfer unit between registers and cache ≤ 1 word (1–16B)
- Data transfer unit between cache and RAM is *cache line*, typically 16–32 bytes, sometimes 128 bytes and more.
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- Each line has associated control info:
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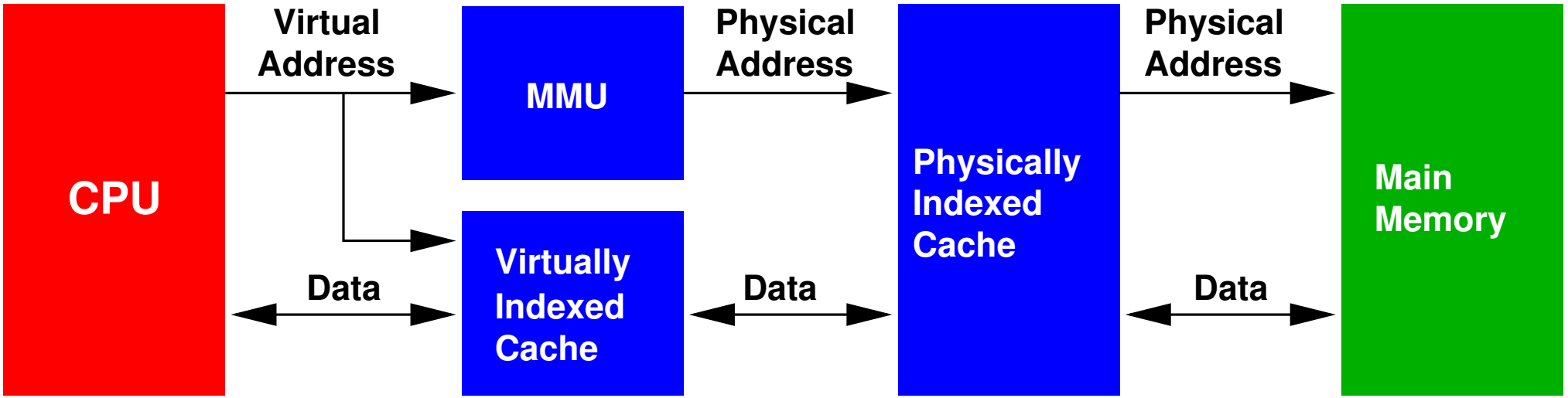
  - ➜ modified bit
  - ➜ tag
- Cache improves memory access by:
  - ➜ absorbing most reads (increases bandwidth, reduces latency),
  - ➜ making writes asynchronous (hides latency),
  - ➜ clustering reads and writes (hides latency).

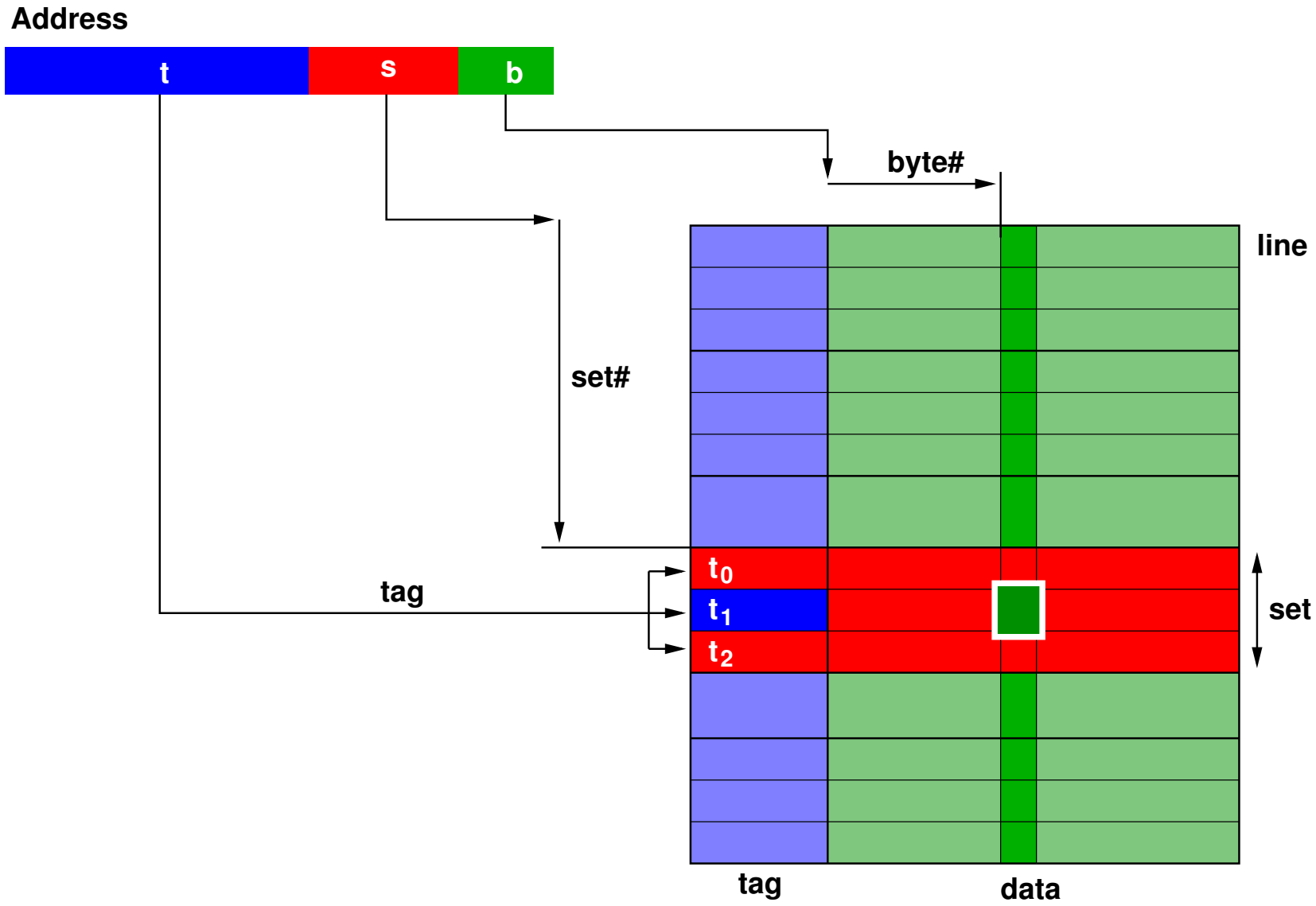
CACHE ACCESS



Virtually indexed: looked up by *virtual address*, operates concurrently with address translation.

Physically indexed: looked up by *physical address*

CACHE INDEXING

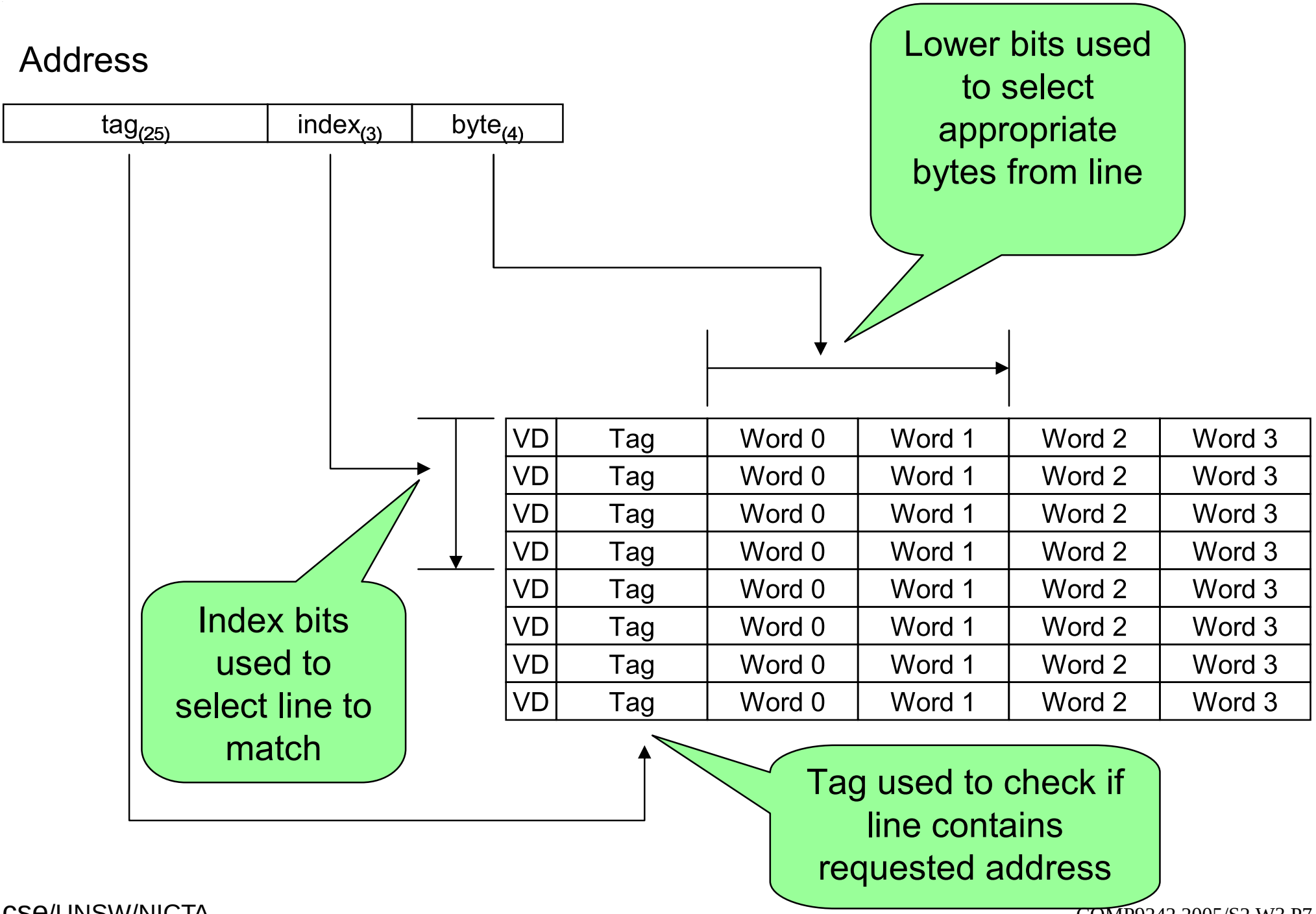


- The *tag* is used to distinguish lines of set...
- ... consists of the address bits not used for indexing.

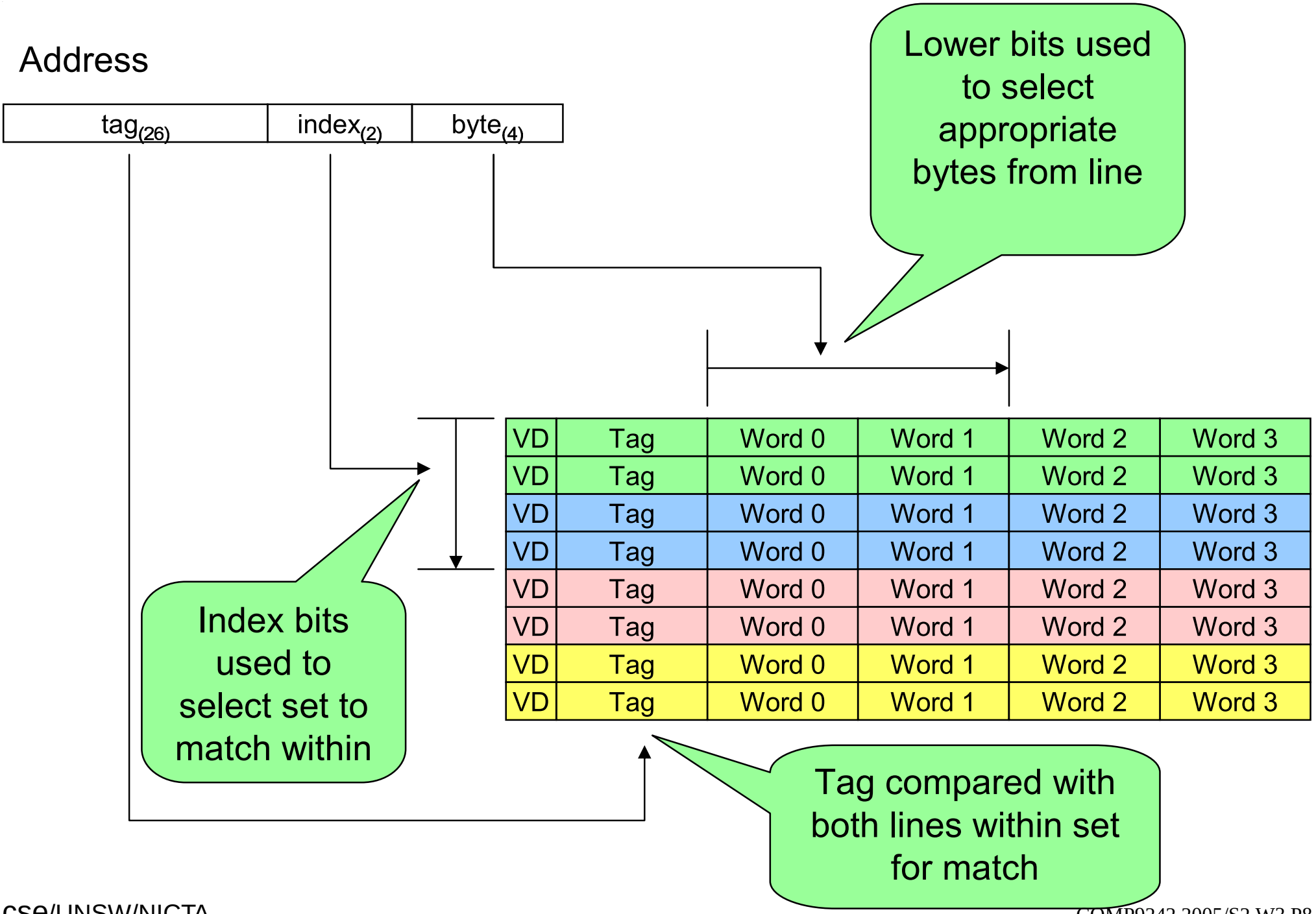
CACHE INDEXING

- Address is hashed to produce index of *line set*.
- Associative lookup of line within set
  n lines per set: *n-way set associative cache*.
  - ⋆ Typically $n = 1 \ldots 5$.
  - ⋆ $n = 1$ is called *direct mapped*.
  - ⋆ $n = \infty$ is called *fully associative*, unusual for CPU caches.
- Hashing must be simple (complex hardware is slow)
  ➜ use least-significant bits of address.

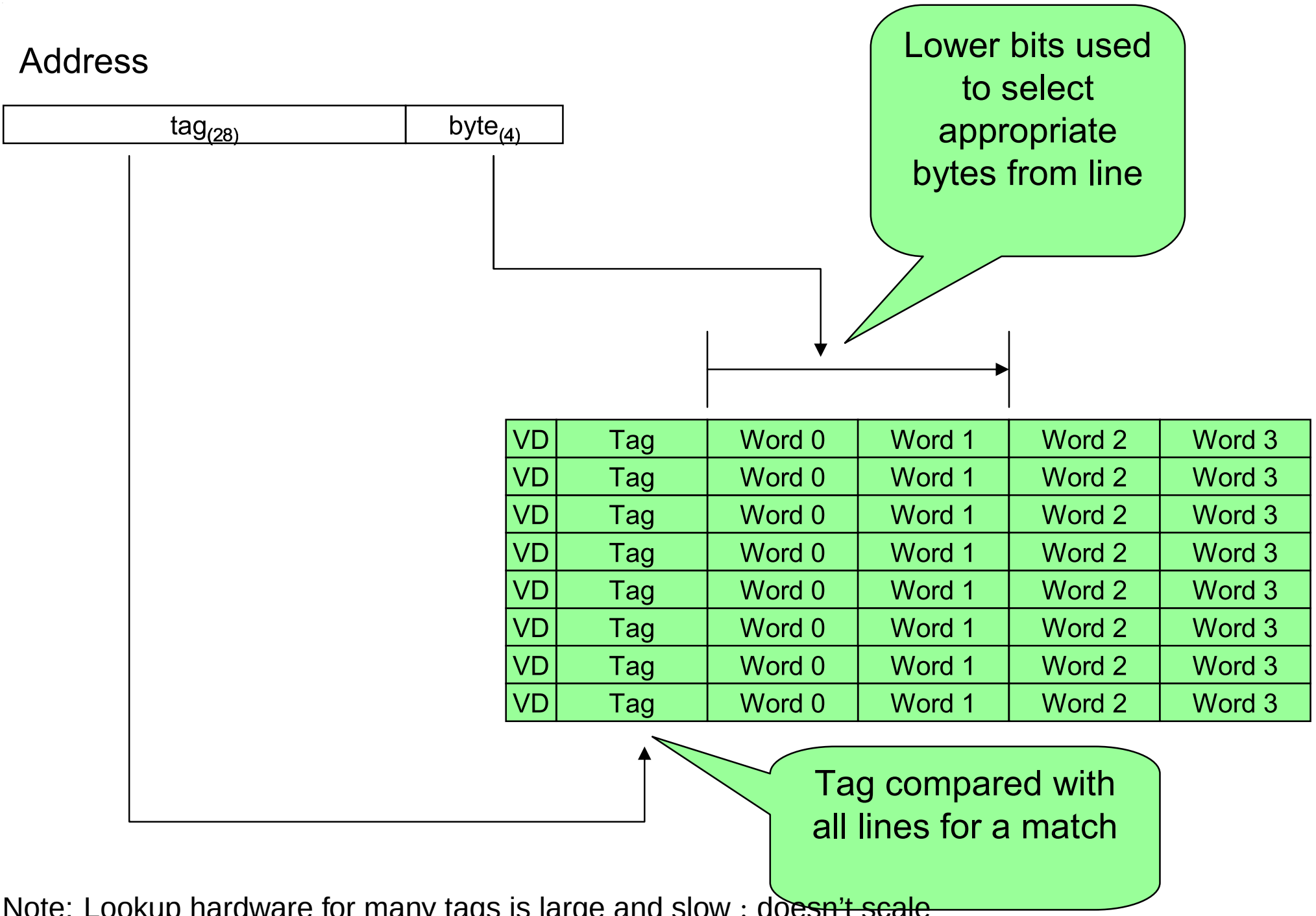
CACHE INDEXING: DIRECT MAPPED



CACHE INDEXING: 2-WAY ASSOCIATIVE



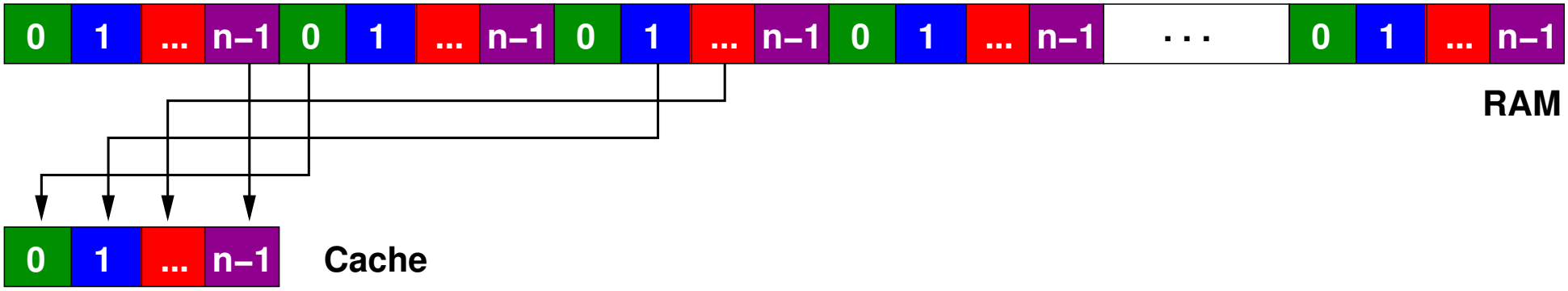
CACHE INDEXING: FULLY ASSOCIATIVE



Note: Lookup hardware for many tags is large and slow : doesn't scale

Cache Mapping

- Different memory locations map to same cache line:



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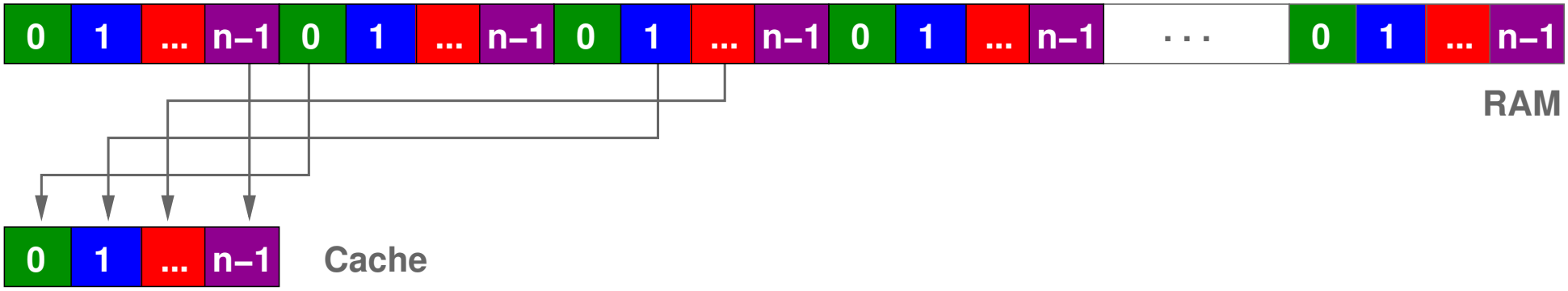

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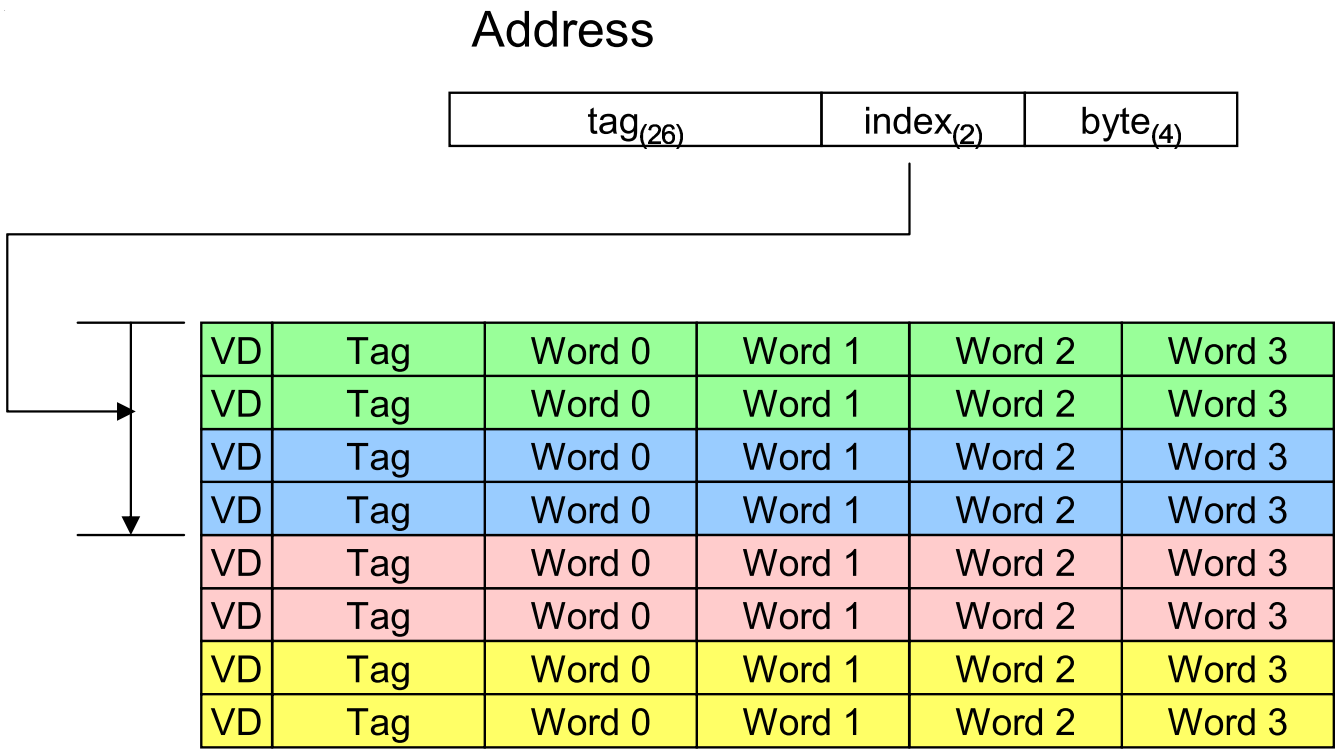
- Types of cache misses:
  - ⋆ **Compulsory miss:** data cannot be in cache (of infinite size)
  - ⋆ **Capacity miss:** all cache entries are in use by other data
  - ⋆ **Conflict miss:** set corresponding to address is full, even though there may be unused lines in the cache.
    - ➜ Cannot occur on fully-associative cache

CACHE REPLACEMENT POLICY

- Indexing (using address) points to specific line set.



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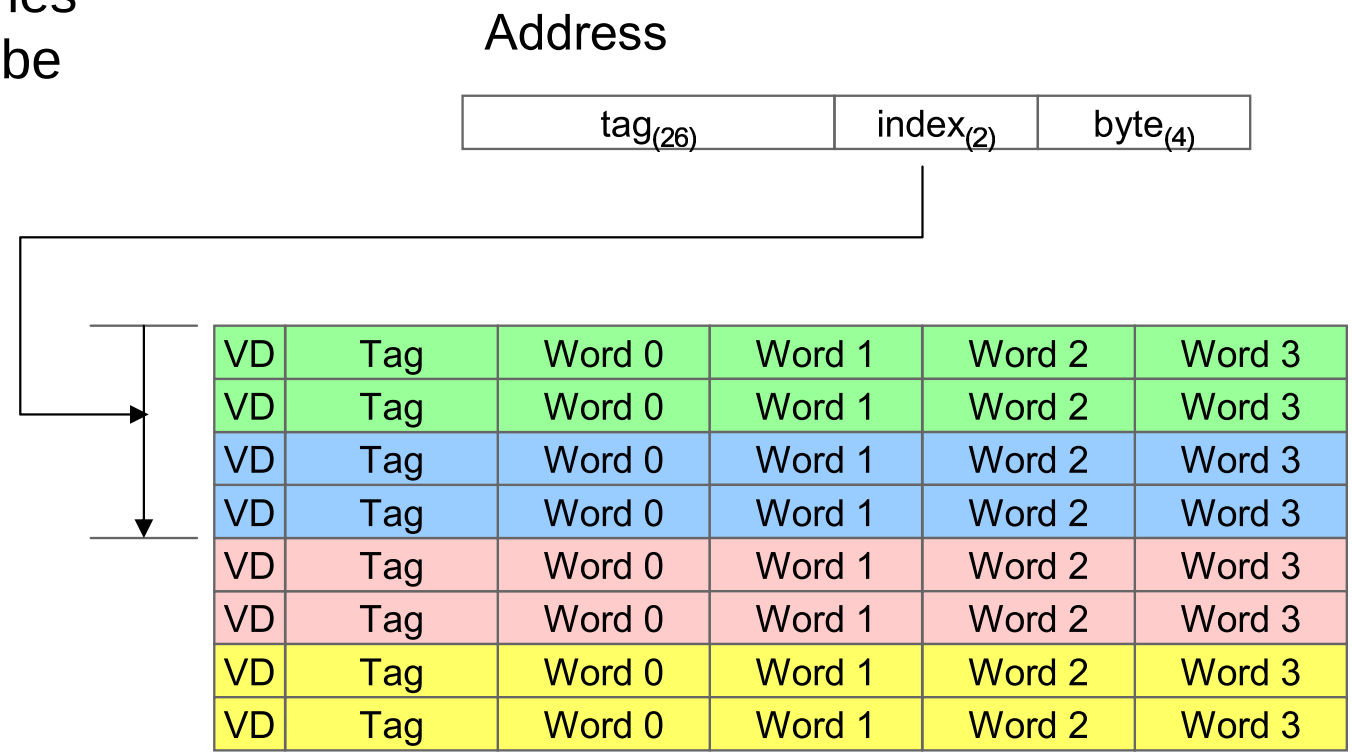
- Replacement strategy must be simple (hardware)

➜ Note: dirty bit determines whether line needs to be written back



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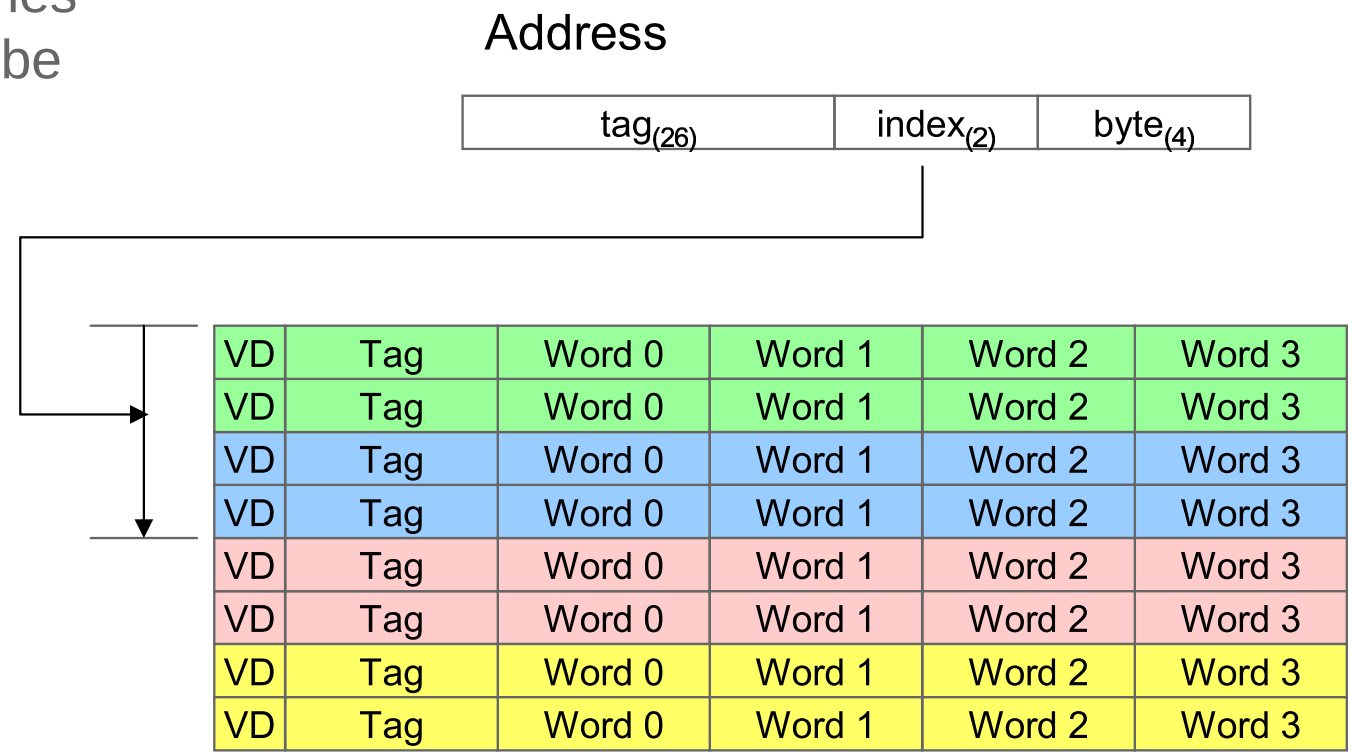
  - ➜ Note: dirty bit determines whether line needs to be written back
- Typical policies
  - ➜ Pseudo-LRU
  - ➜ FIFO
  - ➜ random
  - ➜ toss clean



Cache Write Policy

- Treatment of store operations:
  - ✶ **write back:** Stores only update cache,
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    - ➜ clusters writes
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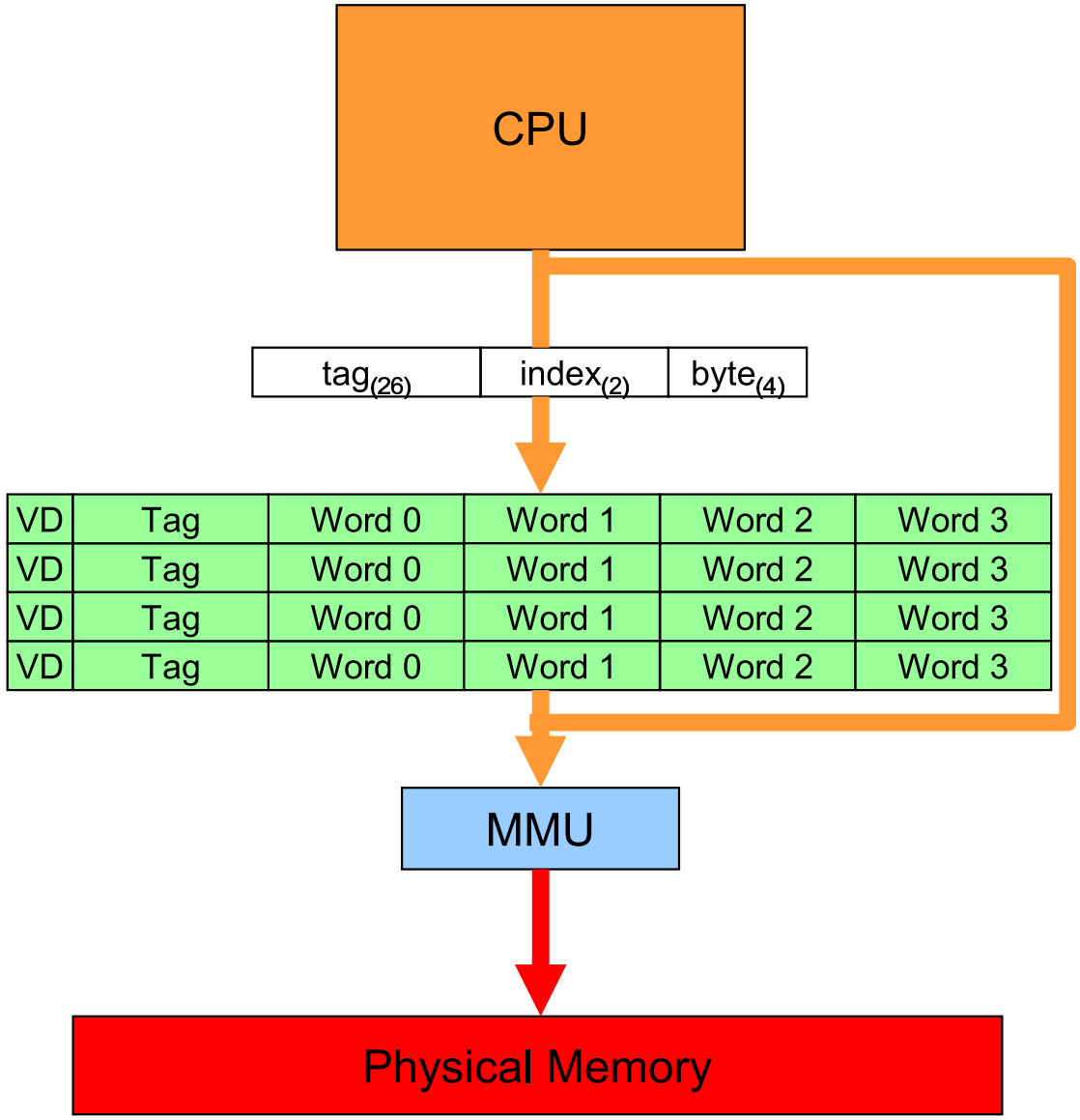
- Usual combinations: write-back & write-allocate,
  write-through & no-allocate.

CACHE TYPES: VV CACHE

VIRTUALLY-INDEXED, VIRTUALLY-TAGGED CACHE

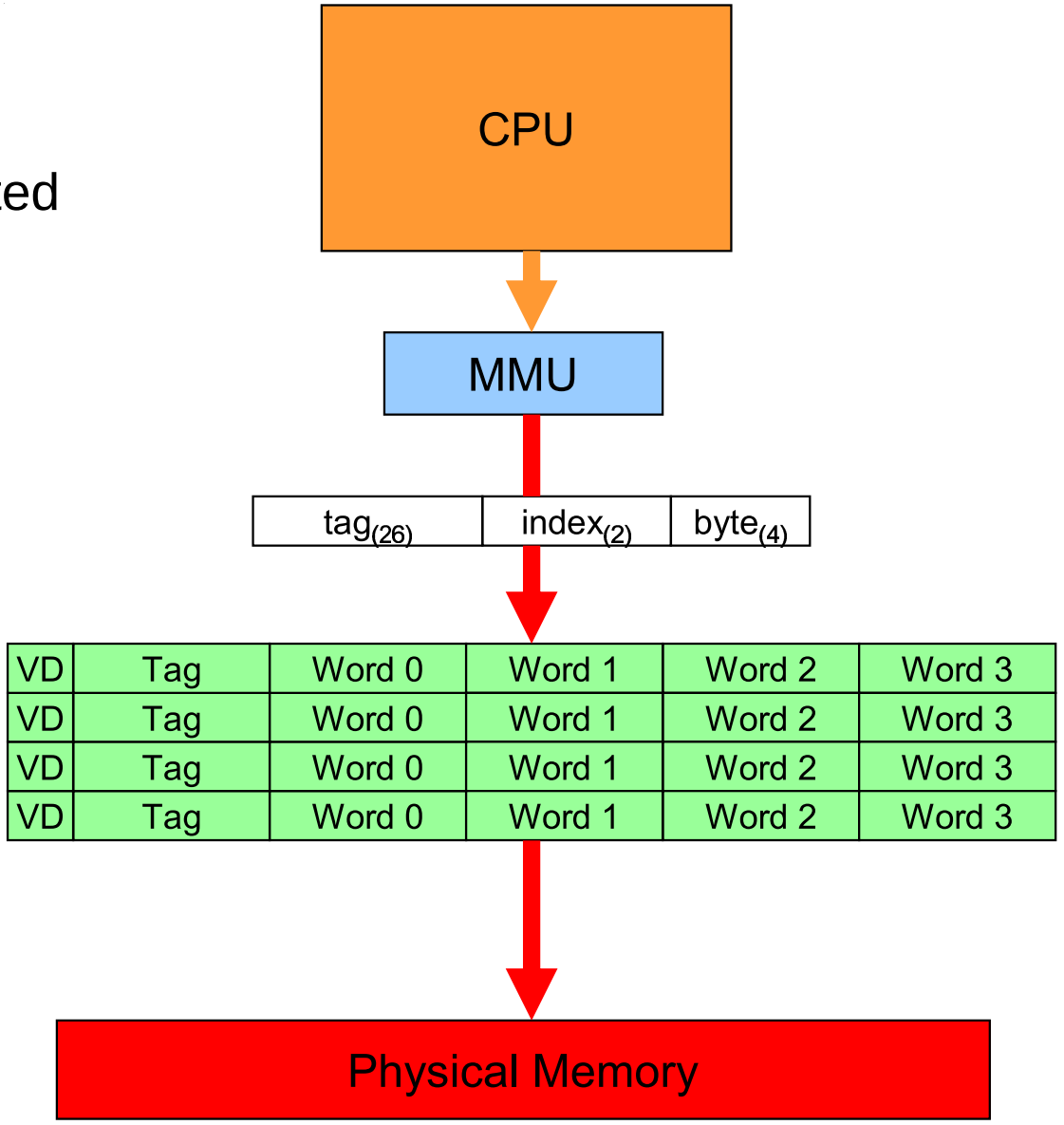
- Also called
  - ➜ virtually-addressed cache
- Also (misleadingly) called
  - ➜ virtual cache
  - ➜ virtual address cache
- uses virtual addresses only
  - ➜ can operate concurrently with MMU
- used on-core



CACHE TYPES: VP CACHE

VIRTUALLY-INDEXED, PHYSICALLY-TAGGED CACHE

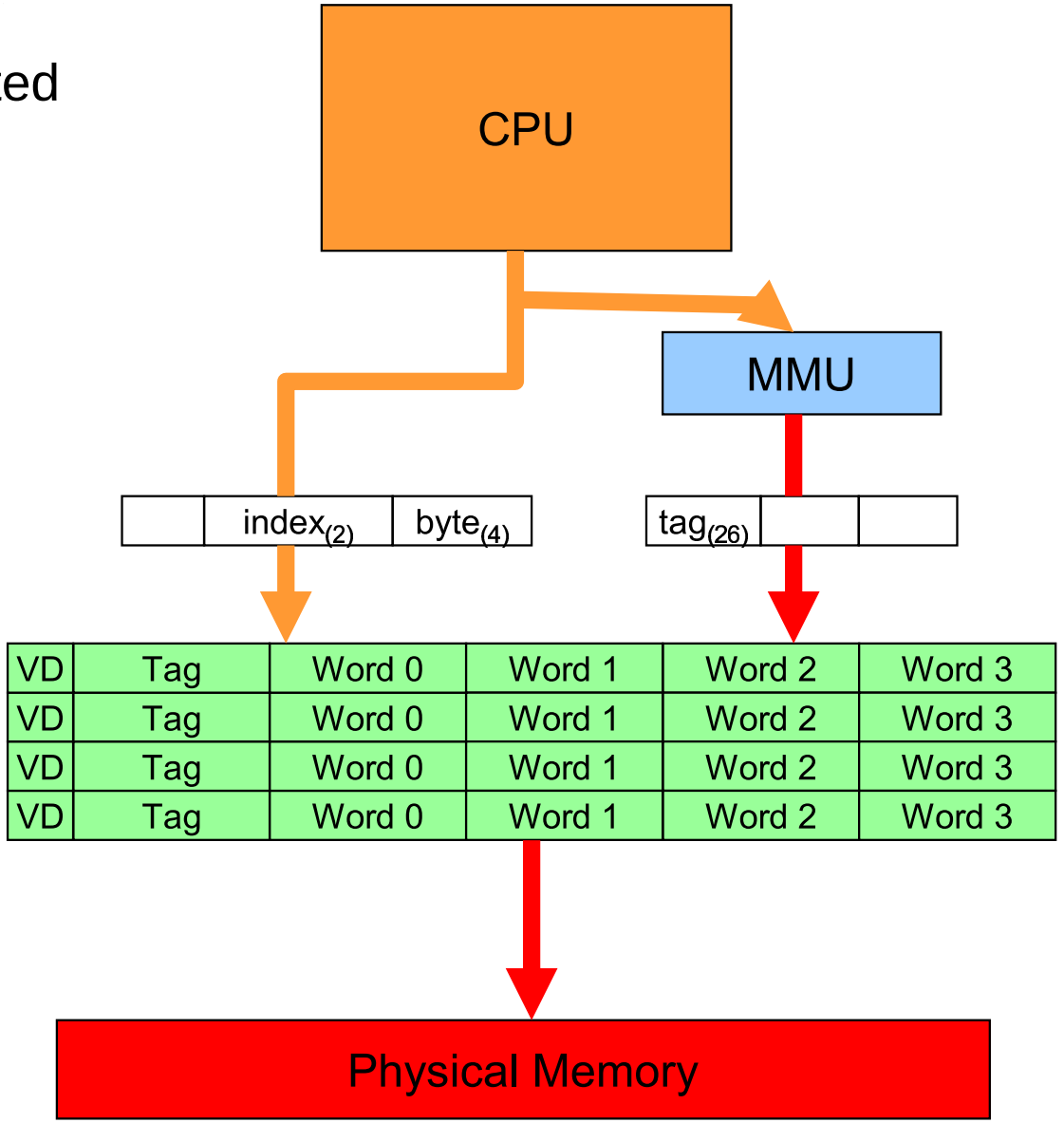
- virtual address for accessing line
- physical address for tagging
- needs address translation completed for retrieving data
- index concurrently with MMU, use MMU output for tag check
- typically used on-core



Cache types: PP Cache

Physically indexed, physically-tagged cache

- only uses physical addresses
- needs address translation completed before begin of access
- typically used off-core



CACHE TYPES: PP CACHE

PHYSICALLY INDEXED, PHYSICALLY-TAGGED CACHE

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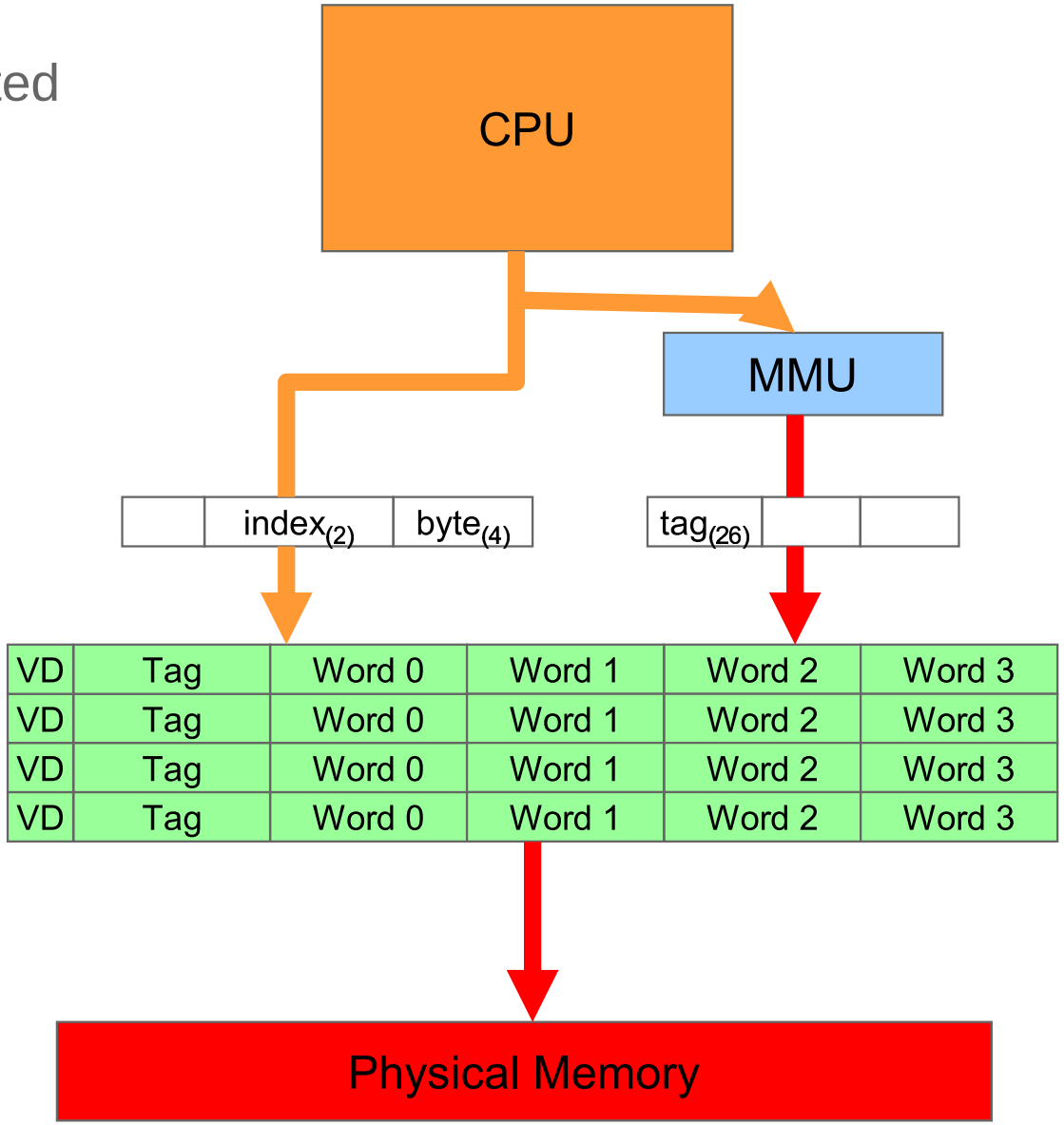
➜ small physically-indexed caches do not require MMU lookup and can be used on-core

➜ details later



Cache Issues

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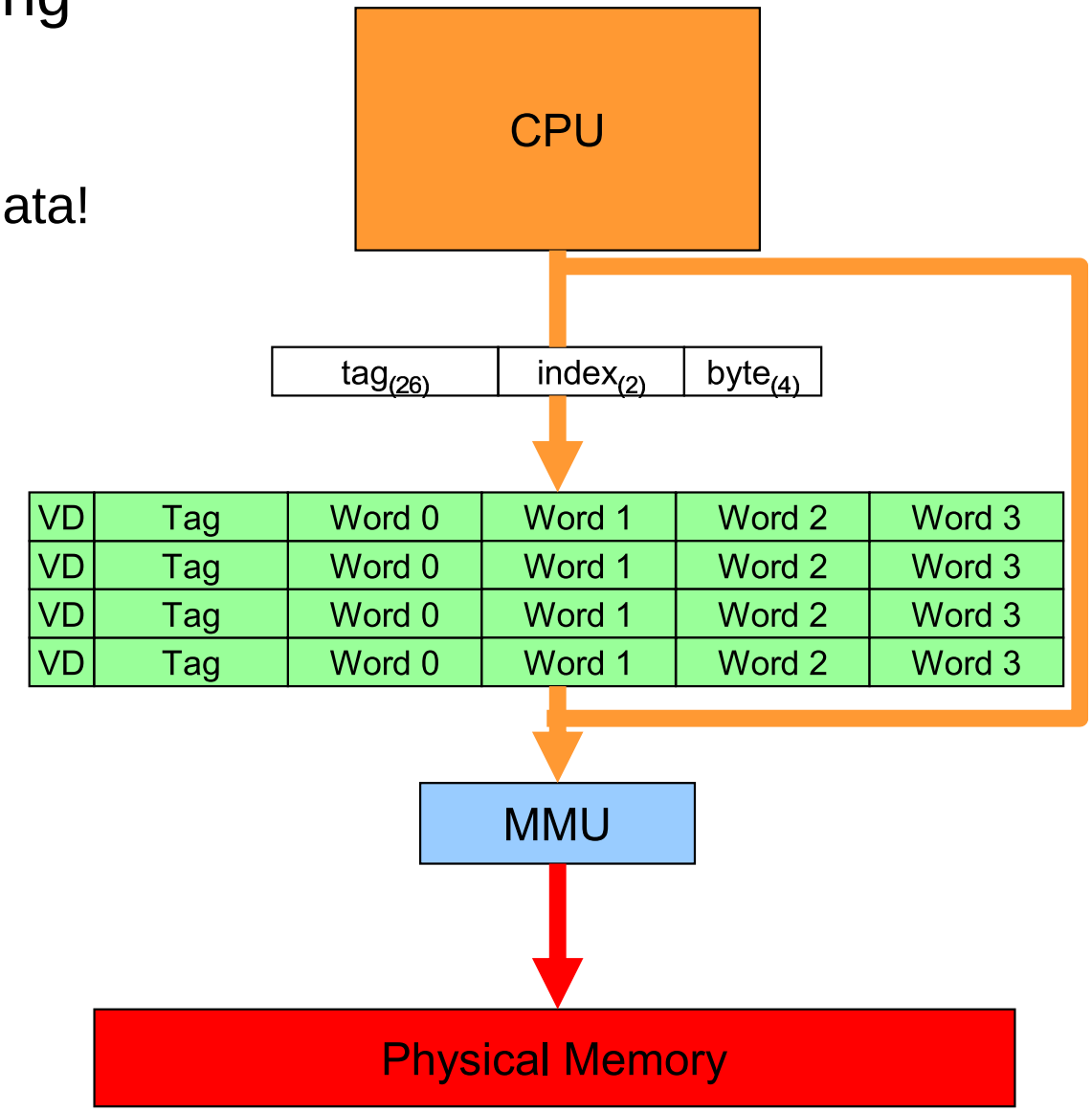
- Software-visible cache effects:
  - ✶ performance
  - ✶ synonyms
    - ➜ can affect correctness!
  - ✶ homonyms
    - ➜ can affect correctness!

VIRTUALLY-INDEXED CACHE ISSUES

HOMONYMS

- Problem: VA used for indexing is context dependent
  - ➜ same VA refers to different PAs
  - ➜ tag does not uniquely identify data!
  - ➜ wrong data is accessed!
  - ➜ an issue for most OS!



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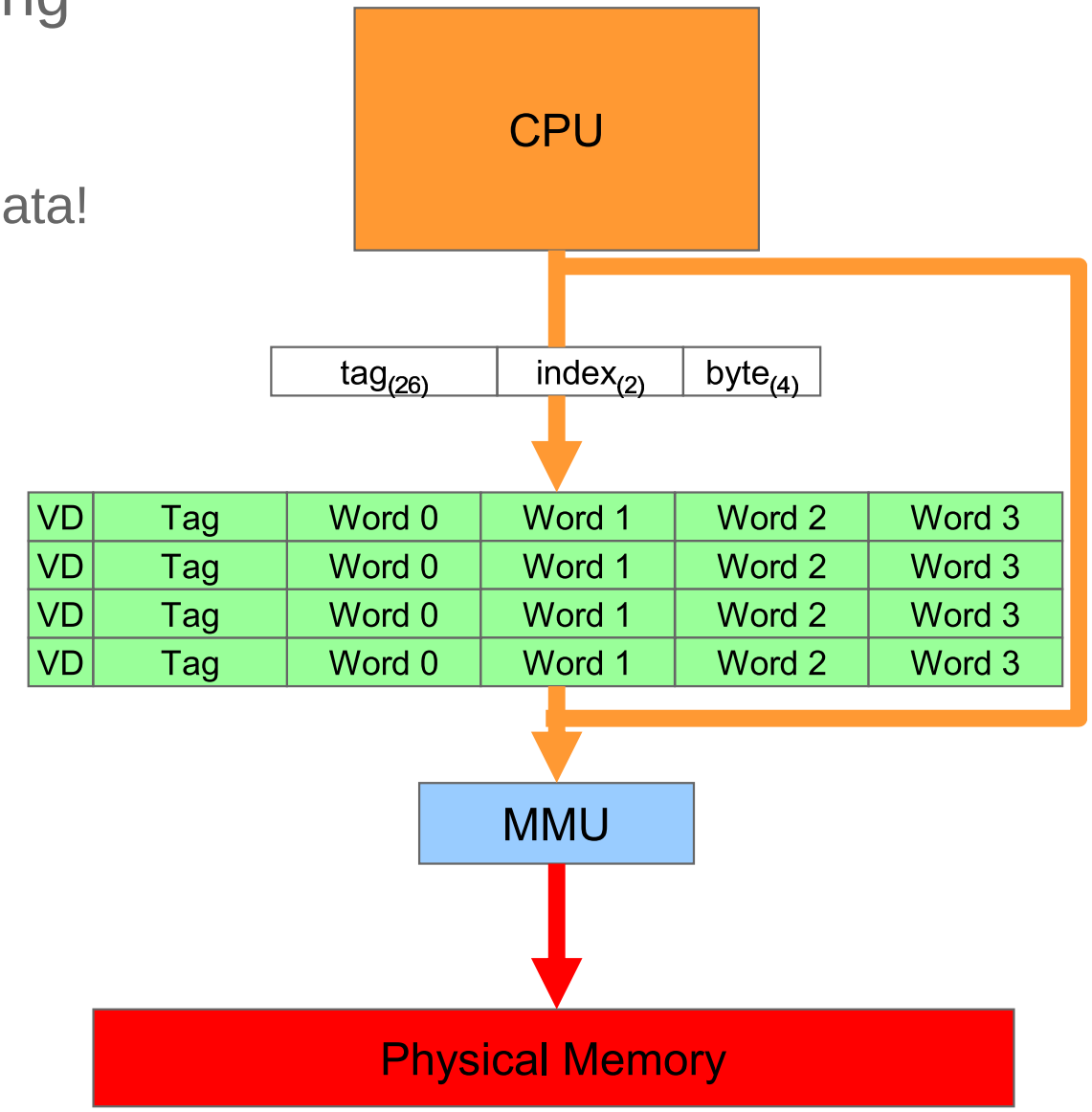
  - ➜ flush cache on context switch
  - ➜ force non-overlapping address-space layout



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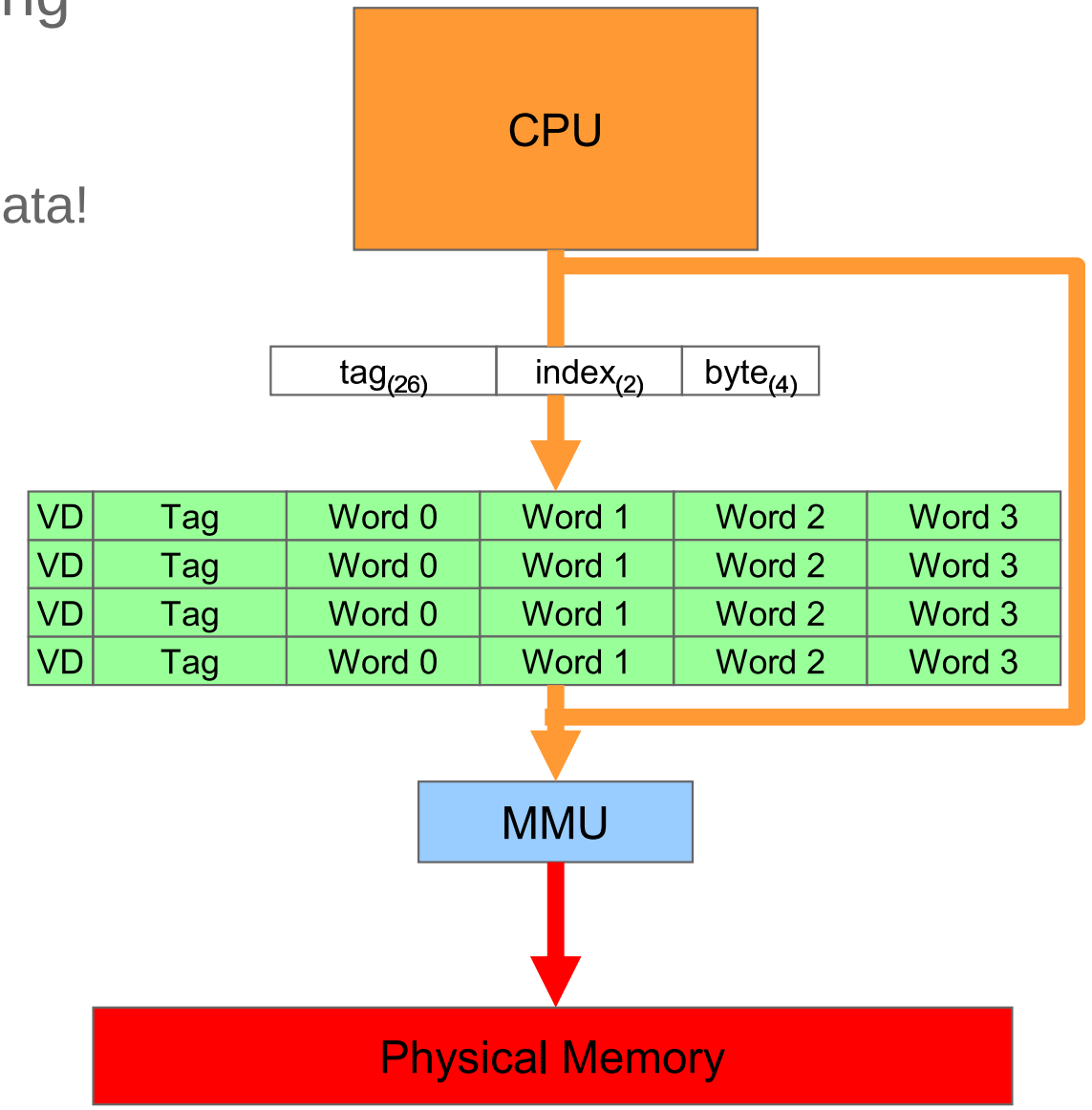
  - ➜ *tag* VA with *address-space ID* (ASID)
    - ➜ makes VAs global
  - ➜ use physical tags



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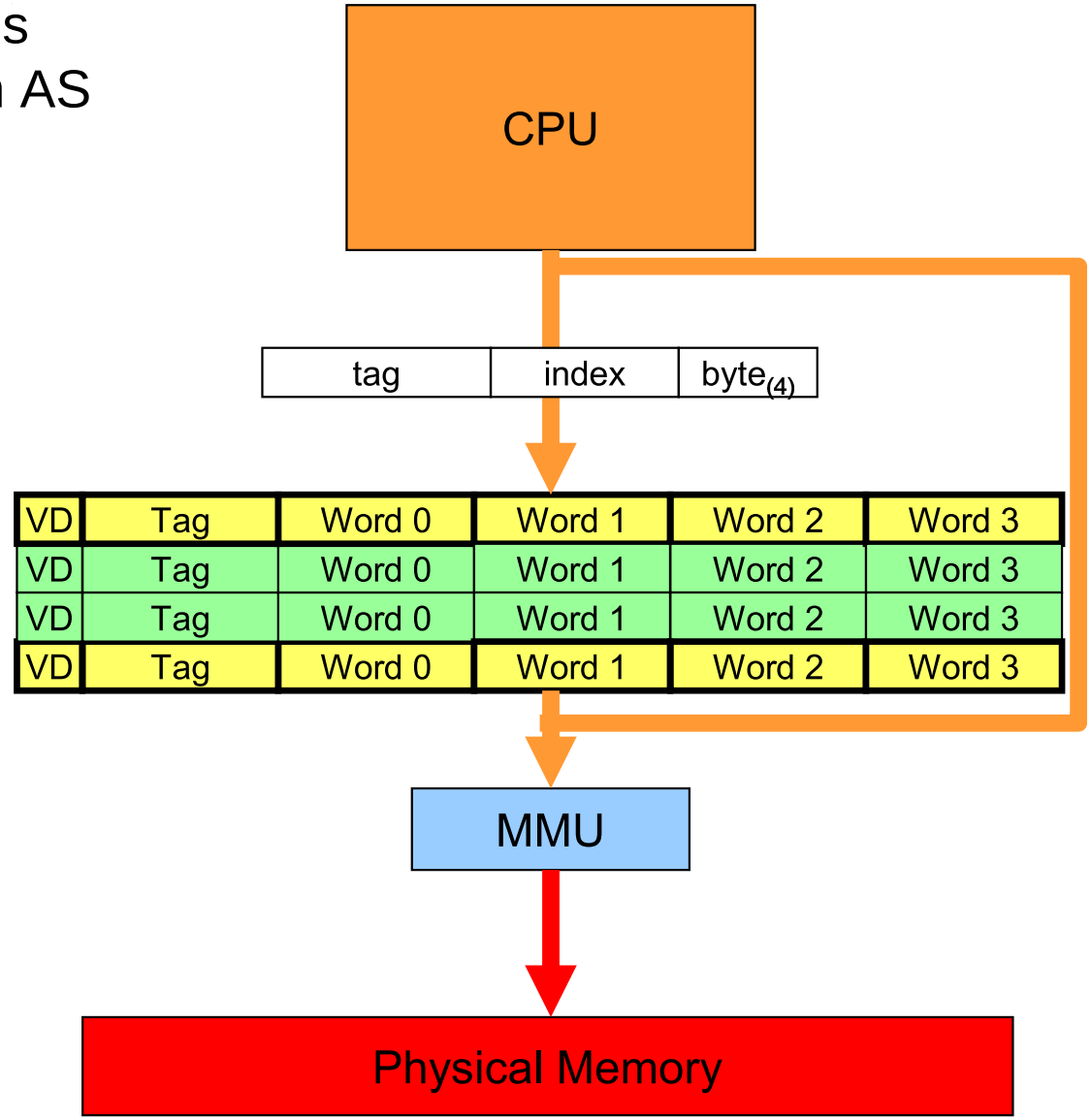
SYNONYMS (ALIASES):

- Several VAs map to the same PA
  - ➜ frames shared between processes
  - ➜ multiple mappings of frame within AS



Virtually-Indexed Cache Issues

Synonyms (Aliases):

- Several VAs map to the same PA
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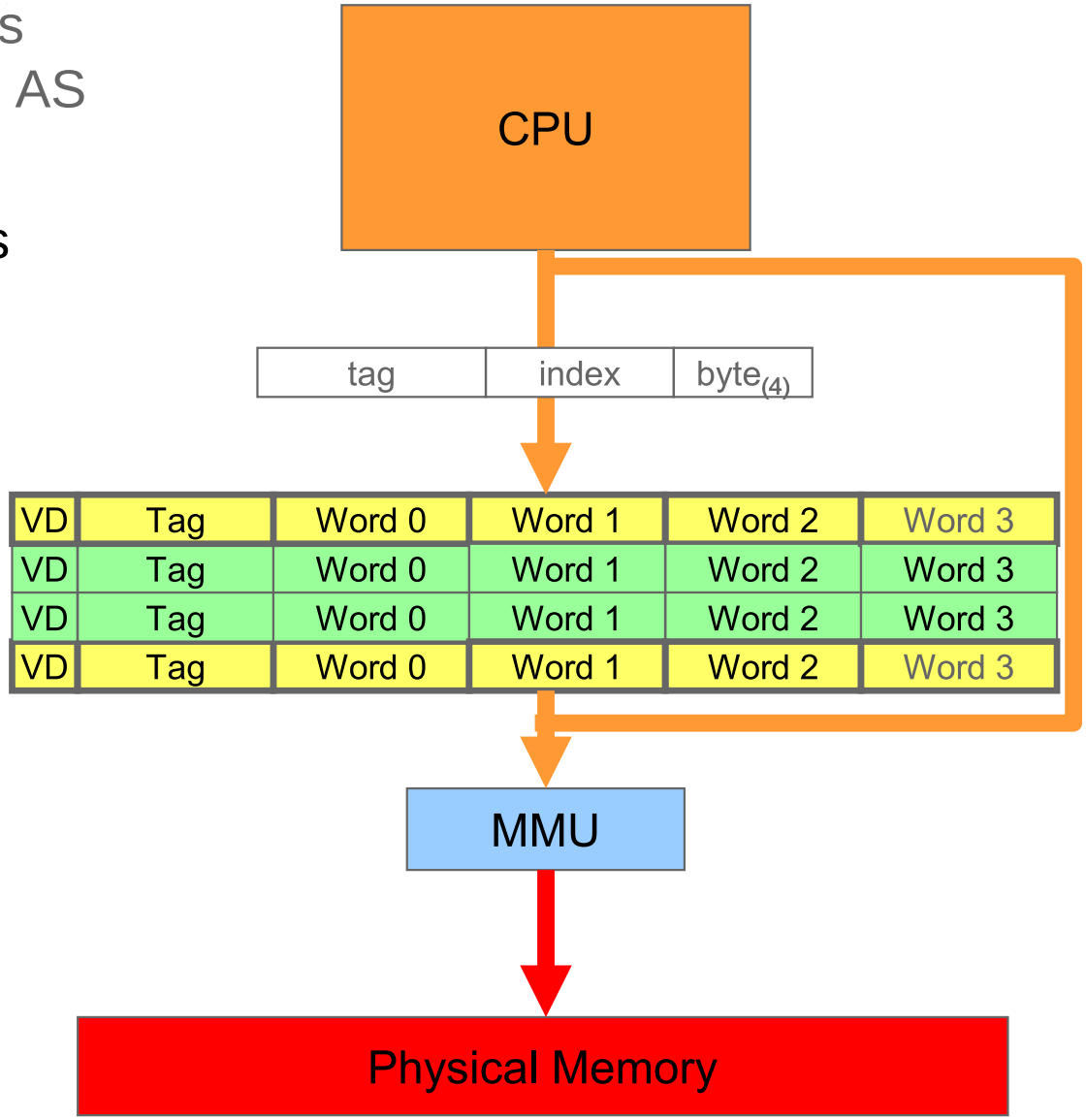
- May access stale data:
  - ➜ same data cached in several lines
  - ➜ on write, one synonym updated
  - ➜ read on other synonym returns old value



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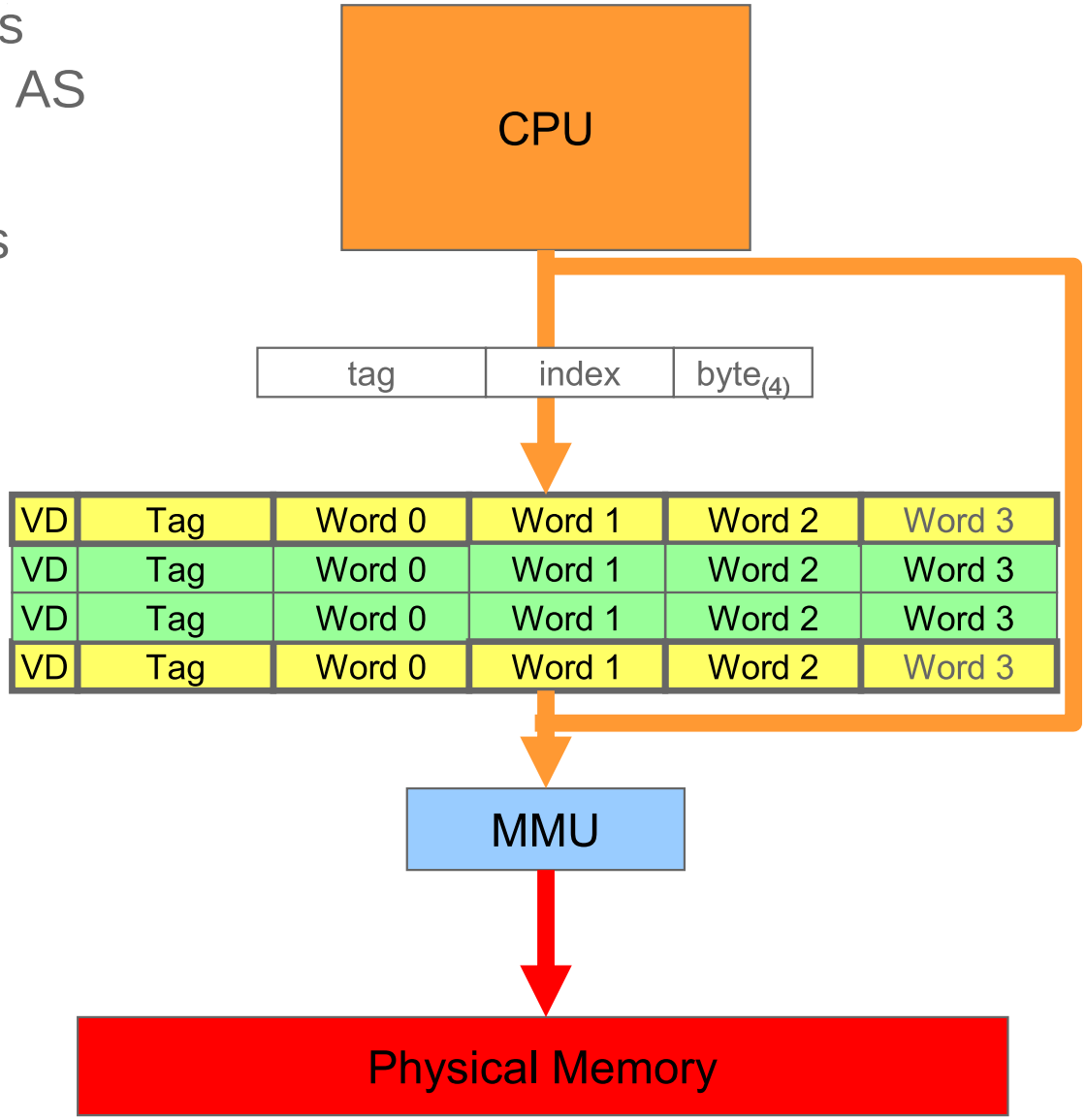
  - ➜ ASIDs don't help



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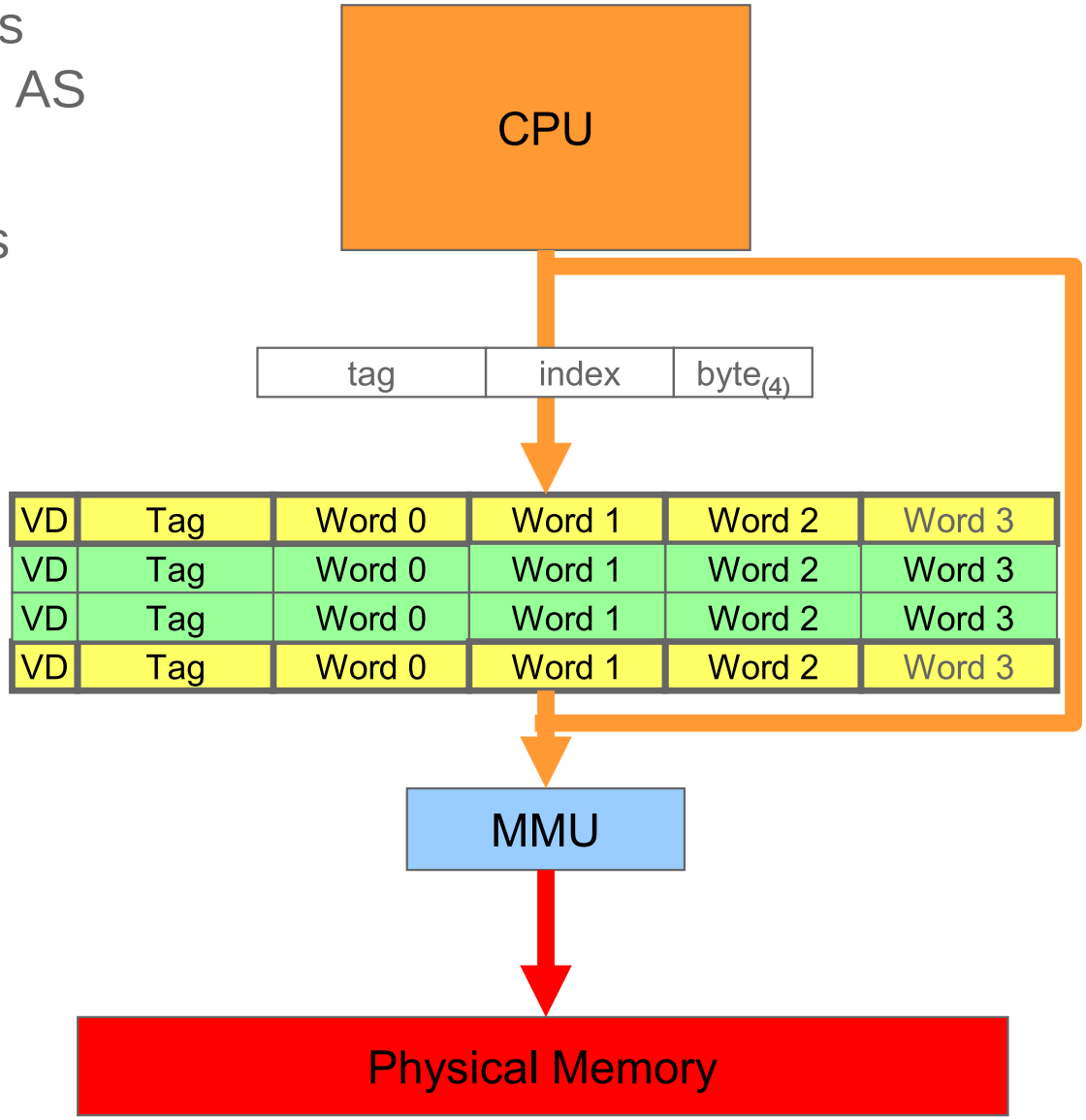
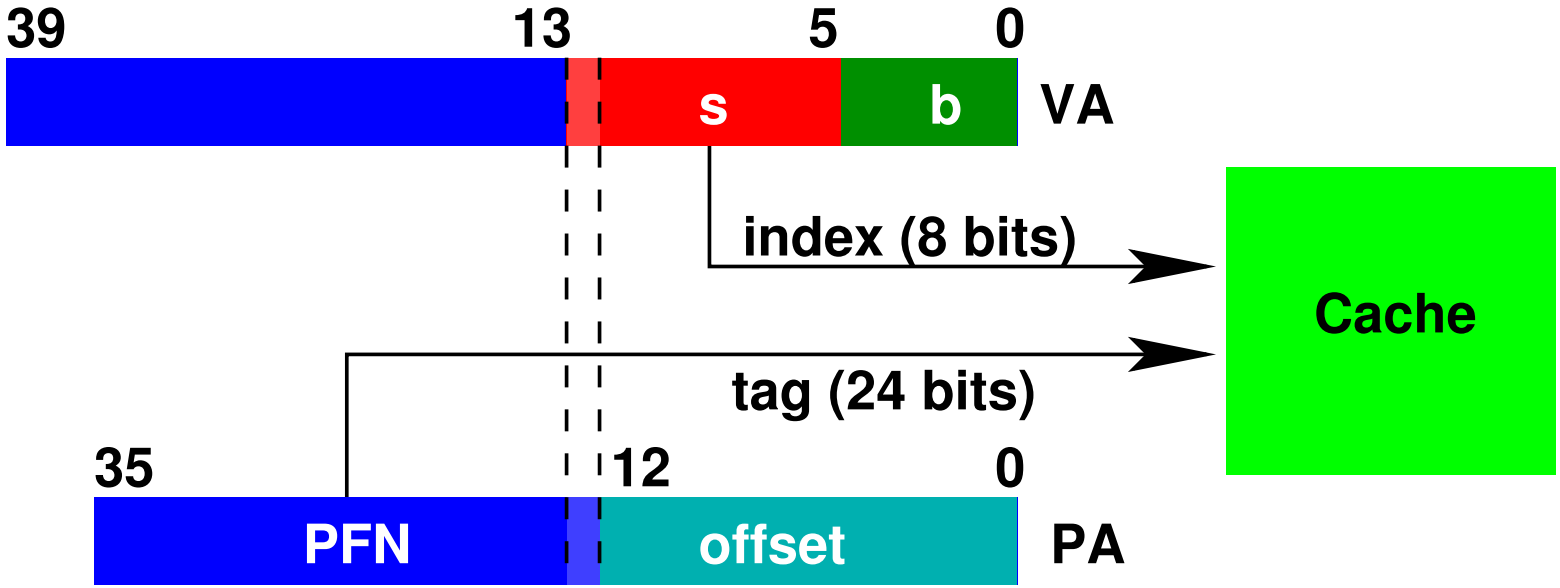
  - ➜ physical tags don't help!
  - ➜ ASIDs don't help
- Are synonyms a problem?
  - ➜ depends on page and cache size
  - ➜ no problem for R/O data or I-caches



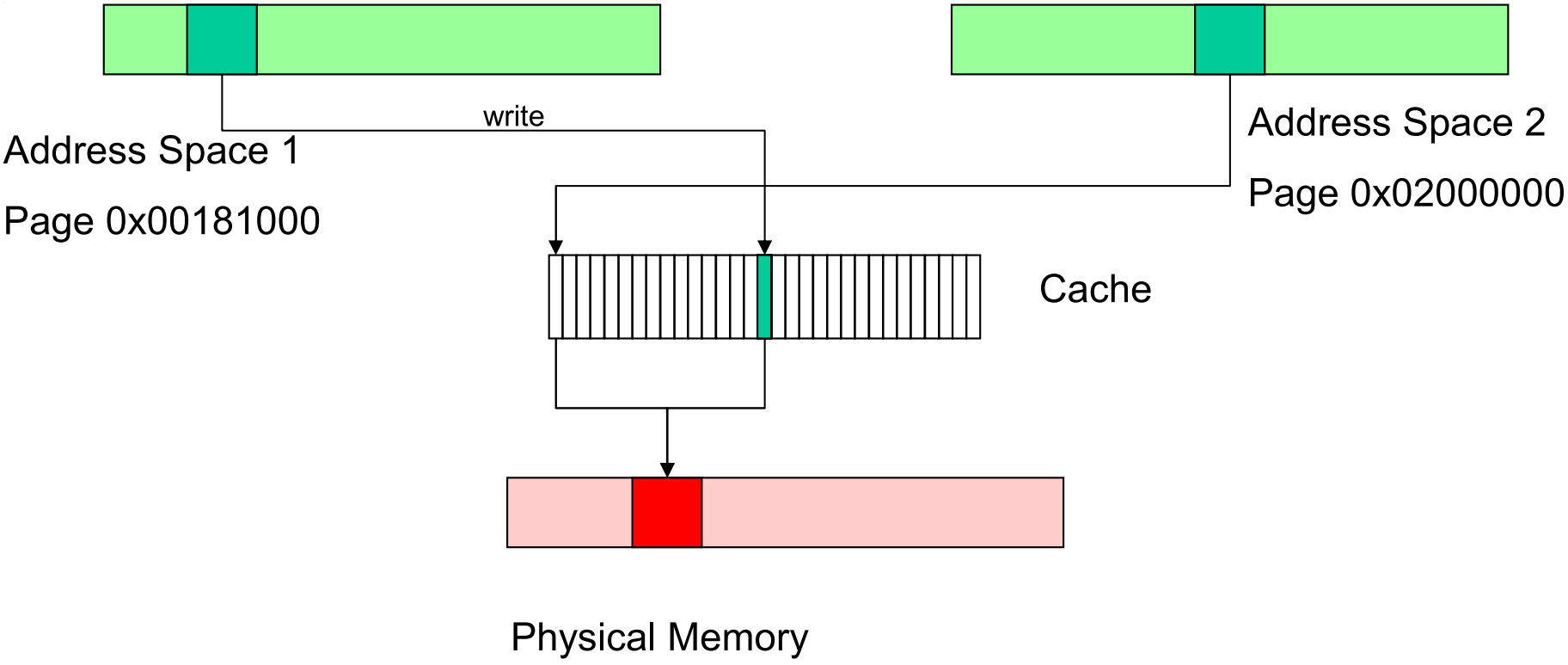
EXAMPLE: MIPS R4X00 SYNONYMS

- ASID-tagged, on-chip L1 VP cache
  - ➜ 16kB cache with 32B lines, 2-way set associative
  - ➜ 4kB (base) page size



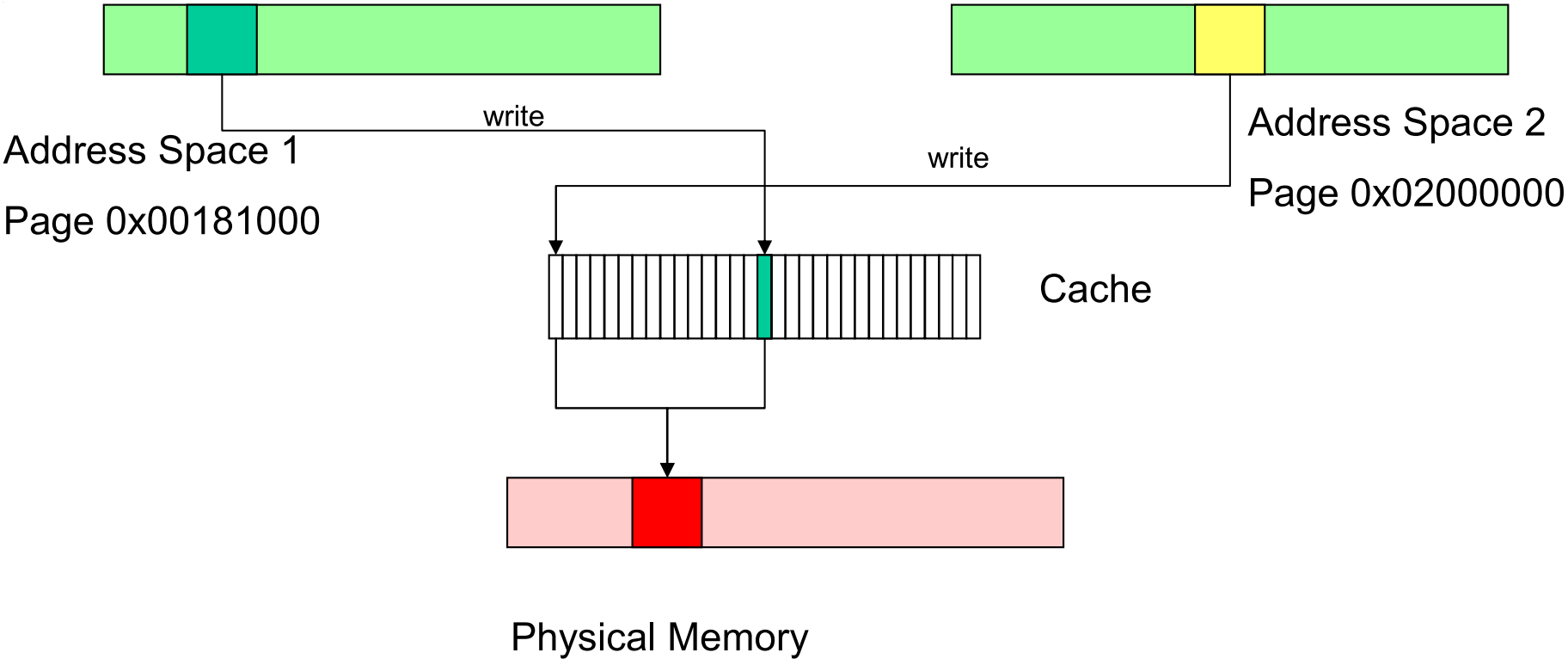
- Remember, location of data in cache determined by index
- Tag only confirms whether it's a hit!
- Synonym problem iff $VA_{12} \neq VA'_{12}$

PROBLEM: ALIASING



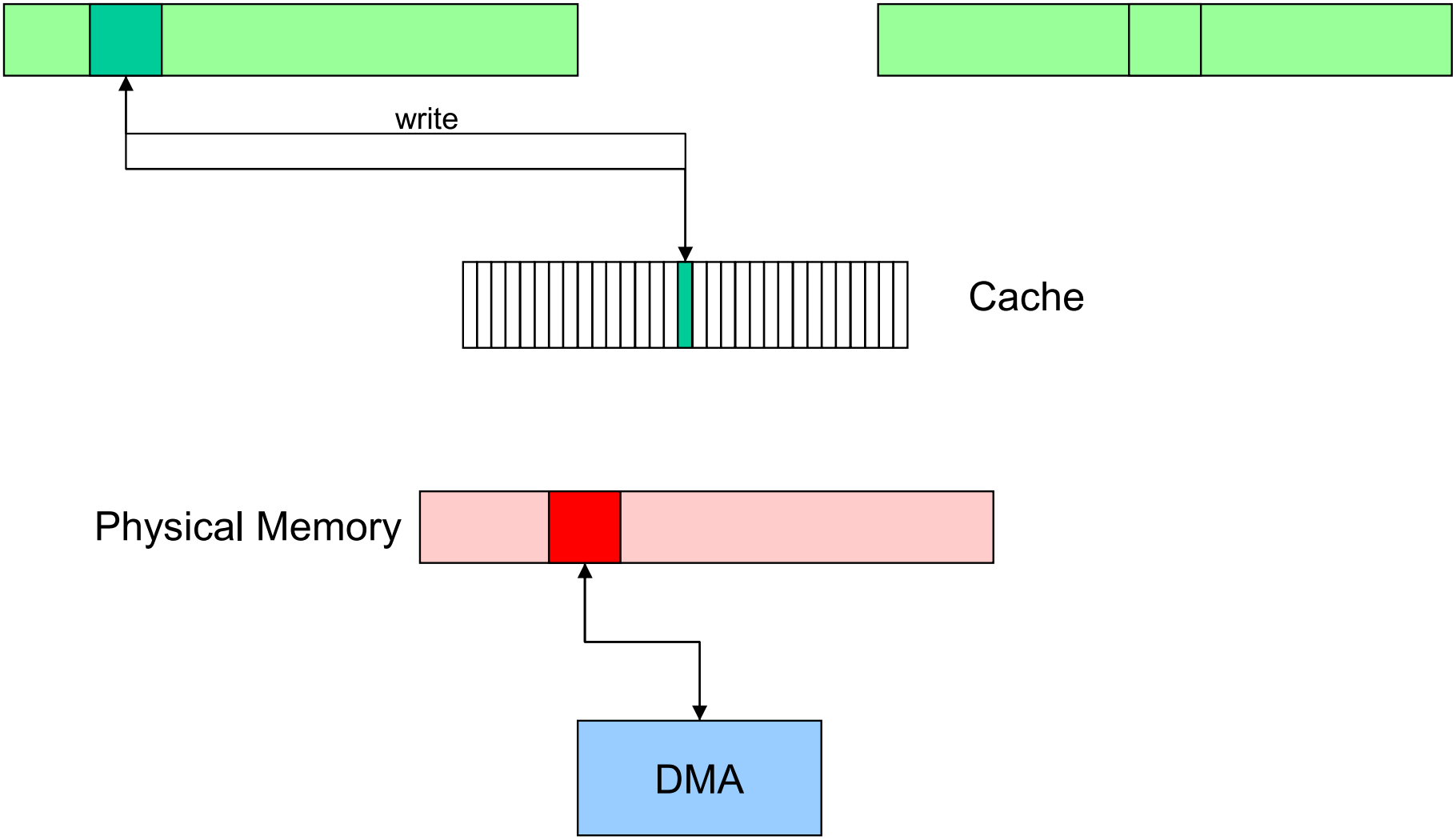
➜ AS_1: $VA_{12} = 1$, AS_2: $VA_{12} = 0$

Problem: Re-Mapping



➜ “Cache bomb”: unaligned orphaned cache line can corrupt memory

Problem: DMA



➜ CPU access inconsistent with device access

SYNONYMS...

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    - ➜ doesn't help for aliasing *within* address space
  - ⋆ detect synonyms and ensure
    - ➜ all read-only, OR
    - ➜ only one synonym mapped
  - ⋆ restrict VM mapping so synonyms map to same cache set
    - ➜ e.g., R4x00: ensure that $VA_{12} = PA_{12}$

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- Fastest (don’t rely on TLB for retrieving data)
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- Require TLB lookup for write-back!
- Used on MC68040, i860, ARMv4/5
- Used for I-caches on a number of architectures
  - ➜ Alpha, Pentium 4, ...

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  - ➜ Potentially better context switching performance
  - ➜ ASID recycling still requires cache flush
- Doesn't solve synonym problem (but that's less serious)
- Doesn't solve write-back problem

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- Medium speed:
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For an in-depth coverage see [Wig03]

Cache Hierarchy

- Use a hierarchy of caches to balance memory accesses:
  - ➜ Small, fast, virtually indexed cache on top (L1 cache).
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- chip multiprocessors (multicores) often share on-chip L2, L3

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- Some architectures (MIPS, Itanium) use a hierarchy of TLBs:
  - ➜ Top-level TLB is hardware-loaded from lower levels.
  - ➜ Transparent to OS.

TLB Issues: Associativity

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  - ➜ Pentium, Pentium-6 (4-way),
  - ➜ IBM RS/6000 (2-way).
- Reasons:
  - ➜ modern architectures tend to support multiple page sizes (superpages)
    - ➜ better utilises TLB entries
  - ➜ TLB lookup done without knowing the page's base address
  - ➜ set-associativity loses speed advantage
  - ➜ superpage TLBs are fully-associative

TLB Size (I-TLB + D-TLB)

Architecture	*TLB Size*	*Page Size*	*TLB Coverage*
VAX	64–256	512B	32–128kB
ix86	32–32+64	4kB+4MB	128–128+256kB
MIPS	96–128	4kB–16MB	384kB–...
SPARC	64	8kB–4MB	512kB–...
Alpha	32–128+128	8kB–4MB	256kB–...
RS/6000	32+128	4kB	128+512kB
Power-4/G5	128	4kB+16MB	512kB–...
PA-8000	96+96	4kB–64MB	
Itanium	64+96	4kB–4GB	

Not much growth in 20 years!

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- The TLB is becoming a performance bottleneck

Address Space Usage vs. TLB Coverage

- Each TLB entry maps one virtual page.
- On TLB miss, reloaded from page table (PT), which is in memory.
  - ➜ Some TLB entries need to map page table.
  - ➜ E.g. 32-bit page table entries, 4kB pages.
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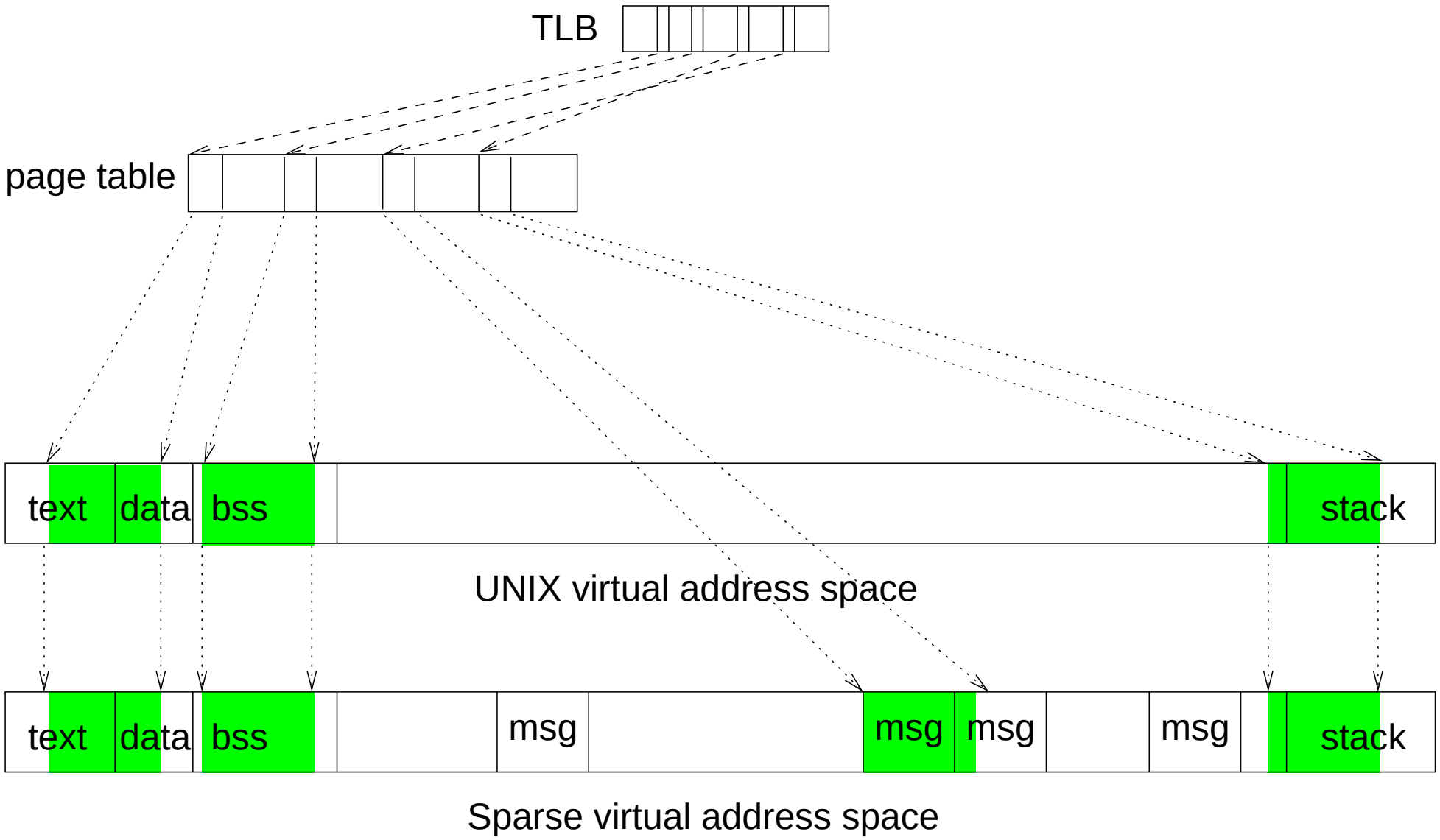
- Traditional UNIX process has 2 regions of allocated virtual address space:
  - ➜ low end: text, data, heap,
  - ➜ high end: stack.
  - ➜2–3 PT pages are sufficient to map most address spaces.
- Superpages can be used to extend TLB coverage
  - ➜ however, difficult to manage in the OS

SPARSE ADDRESS SPACE USE TIES UP PT ENTRIES



Origins of sparse address-space use

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- Modern OS features:
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  - ➜ dynamically-linked libraries,
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- This problem gets worse 64-bit address spaces:
  - ➜ bigger page tables.
- An in-depth study of such effects can be found in [UNS+94].

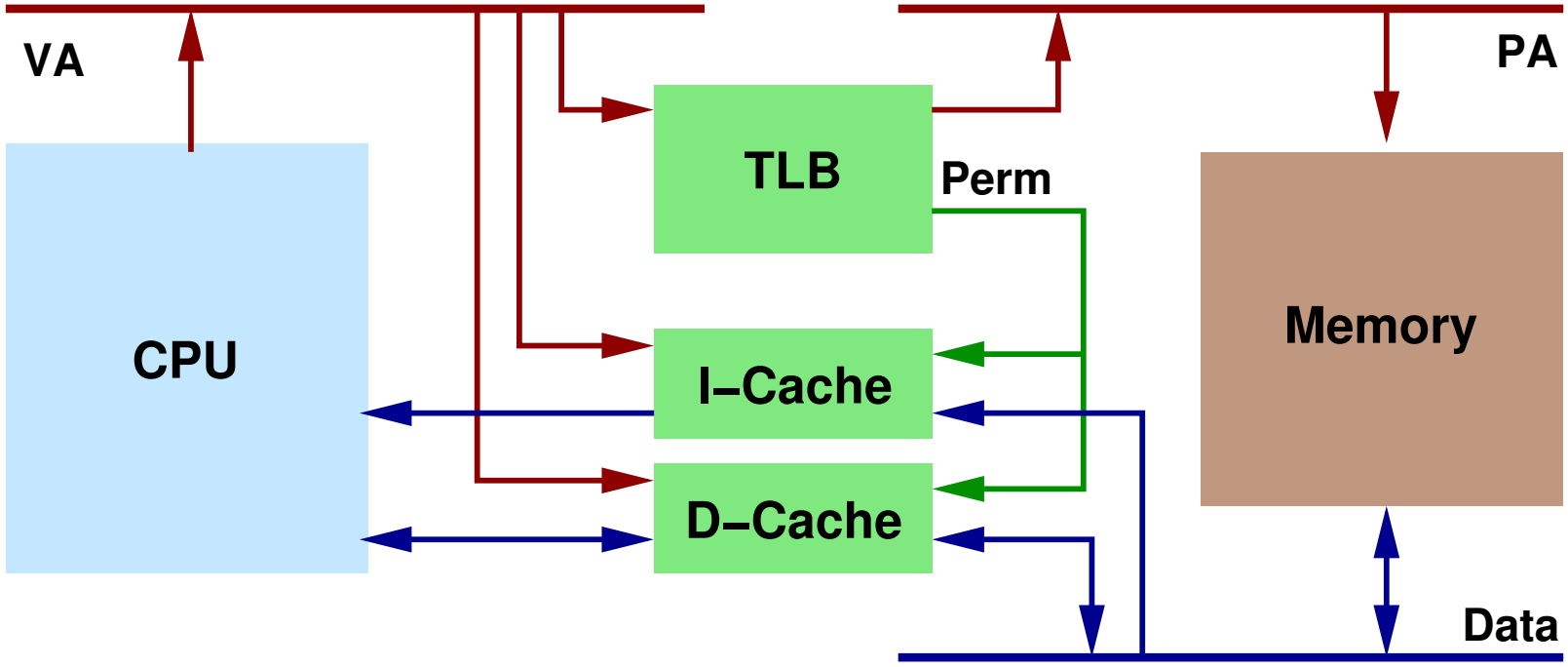
CASE STUDY: CONTEXT SWITCHES ON ARM

ARM FEATURES:

- Virtually-indexed caches
- No address-space TLB tags
- Shared pages

The following is from [WTUH03]

ARM Cache Architecture



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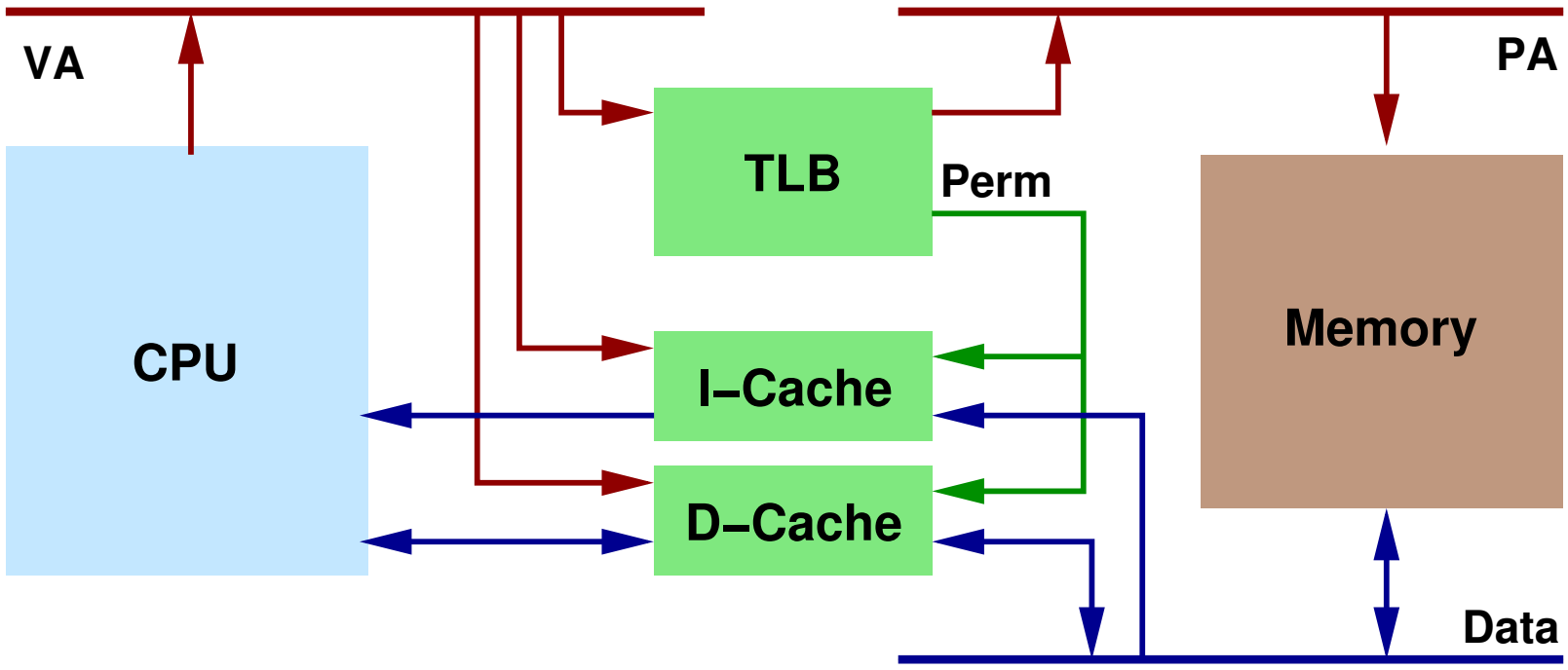

Virtually-indexed caches:

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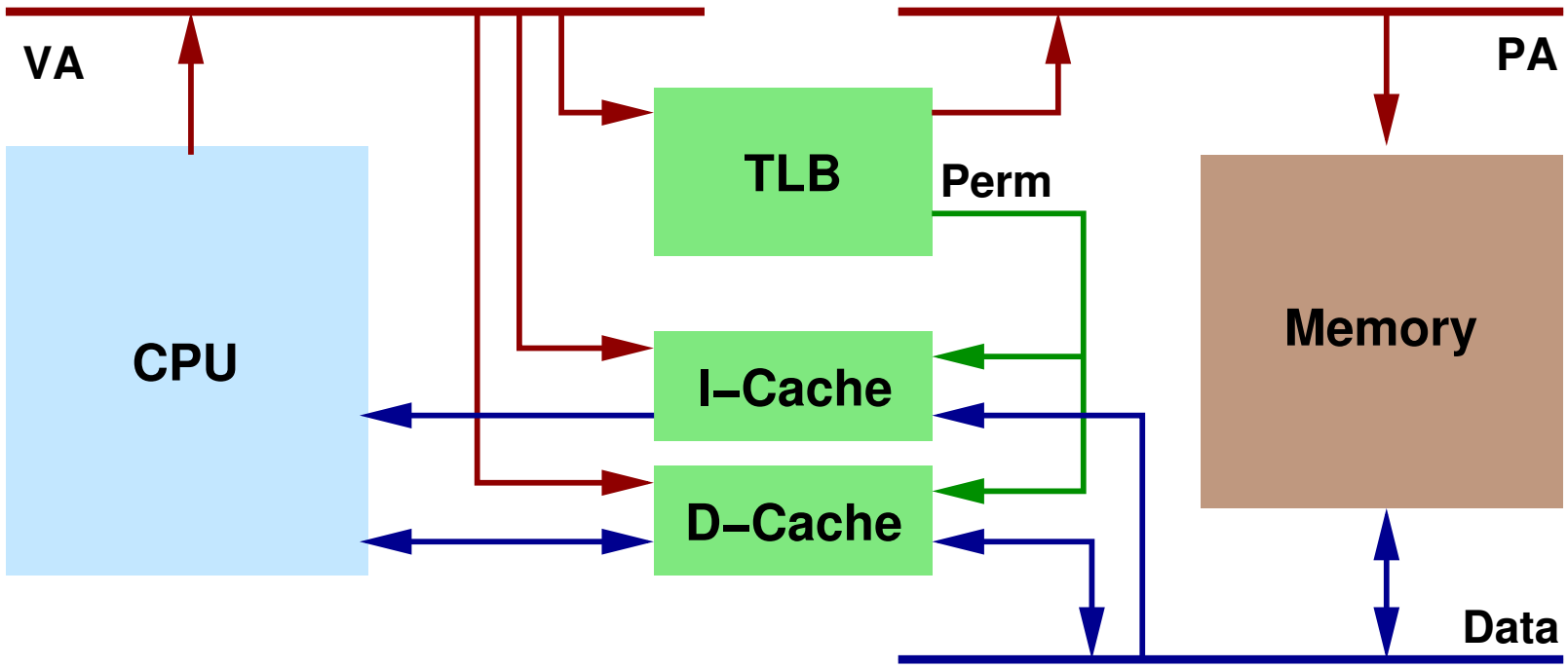

Virtually-indexed caches:

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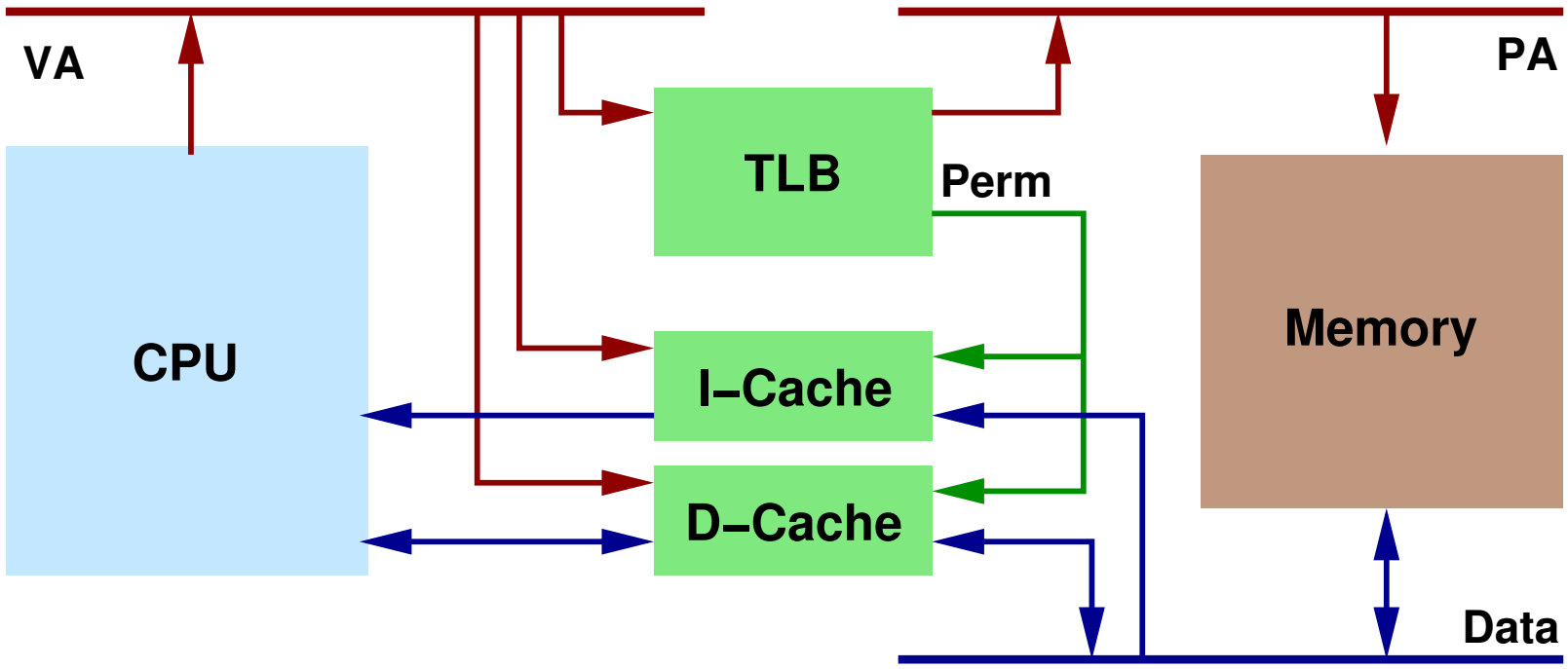

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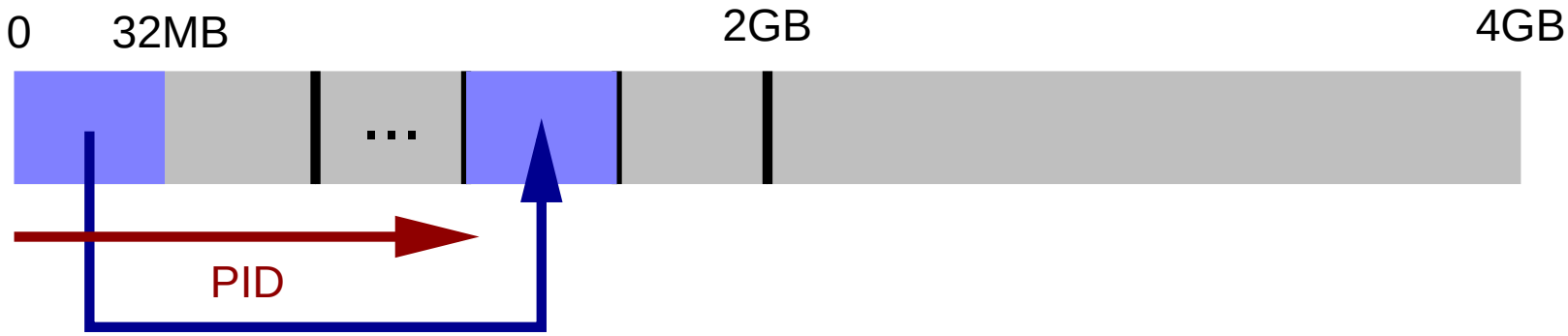
Permissions from TLB lookup:

- ➜ could avoid flushes if no address-space overlap
- ➜ unfeasible in standard OS

StrongARM PID Relocation

- Processor supports relocation of small address spaces:
  - ➜ lowest 32MB gets remapped into lower half of address space

StrongARM PID Relocation



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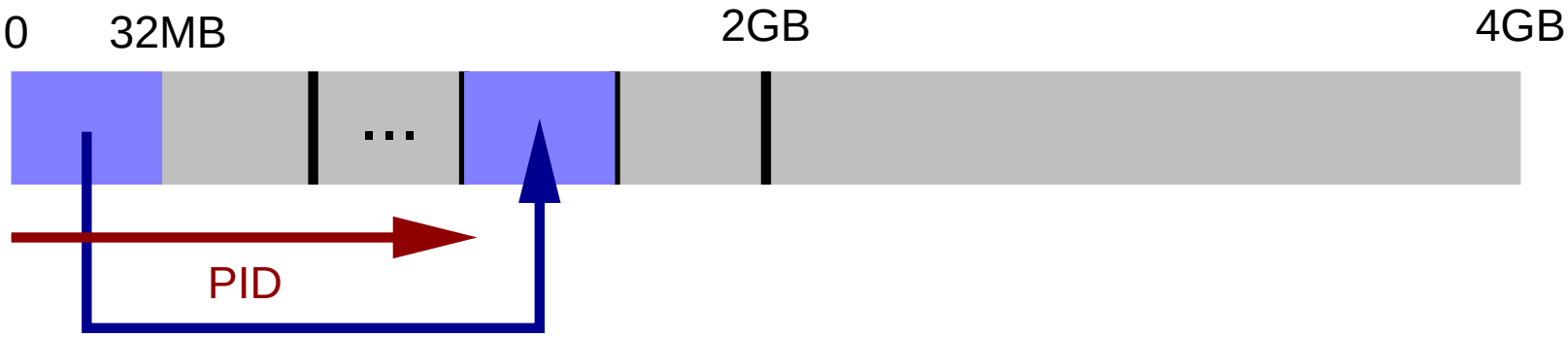

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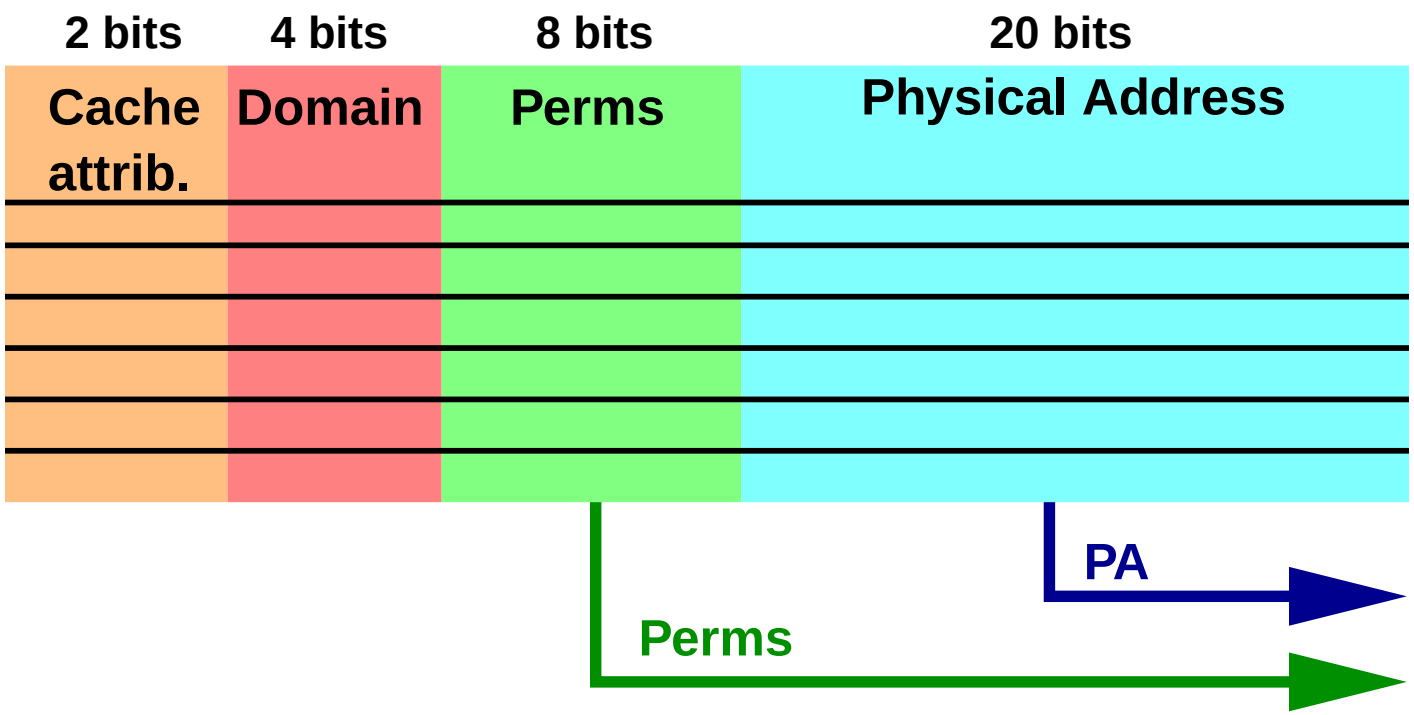
- Re-mapped address spaces don't overlap:
  - ➜ no need to flush caches on address-space switch
  - ➜ used by Windows CE

ARM TLB

- TLB has no PID tag



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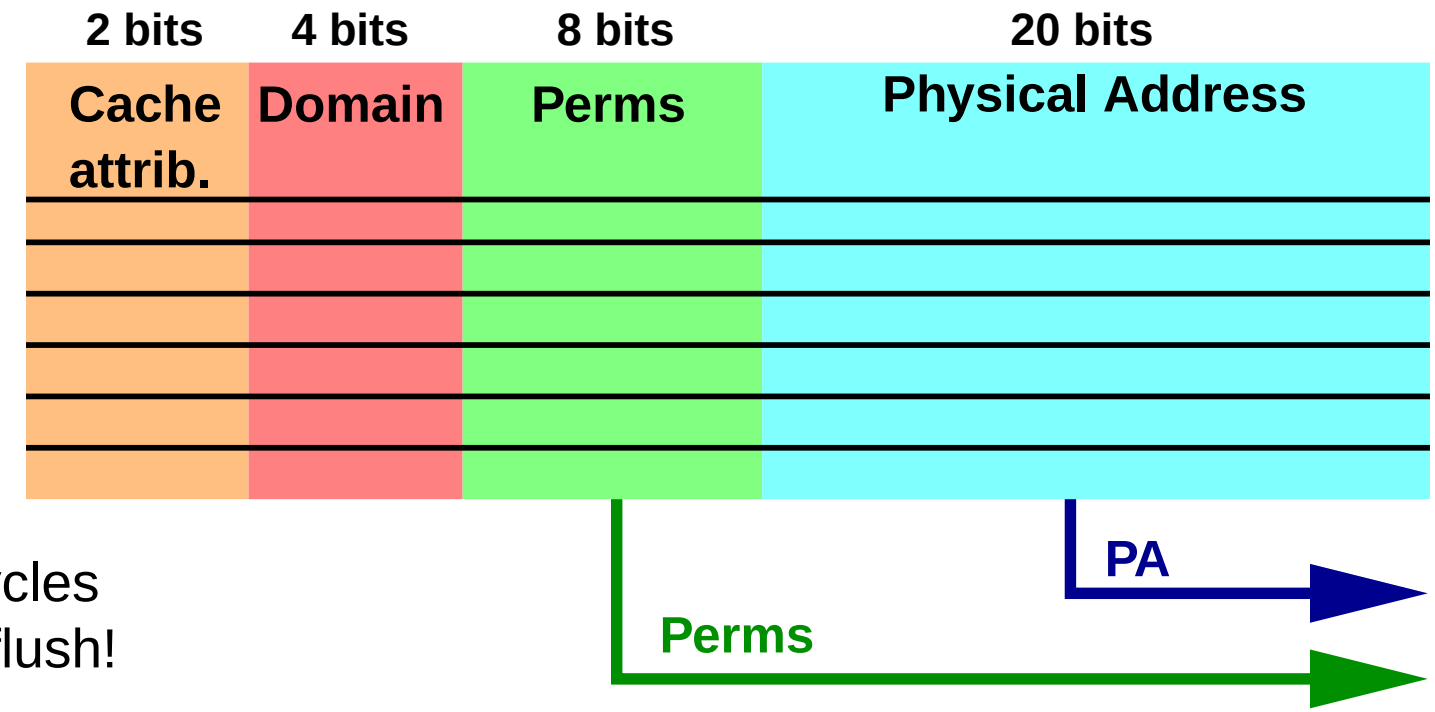

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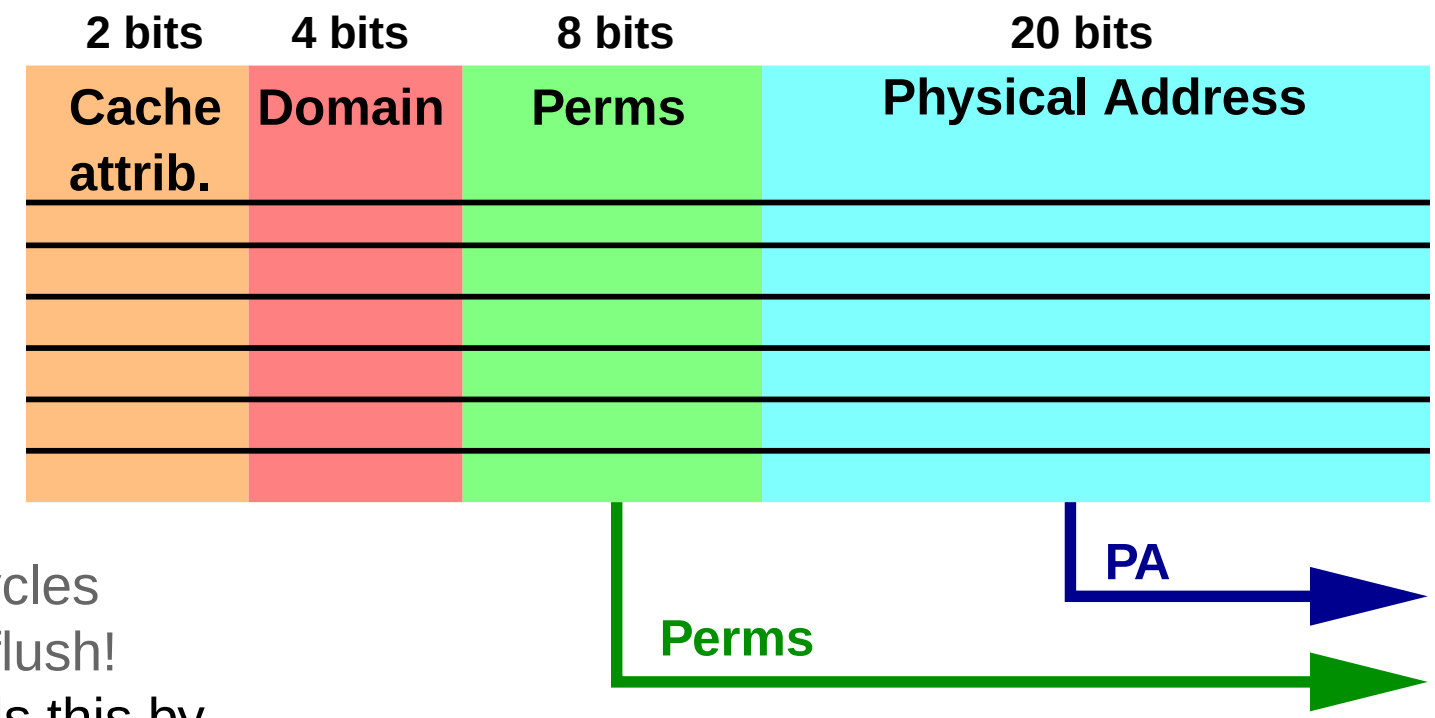

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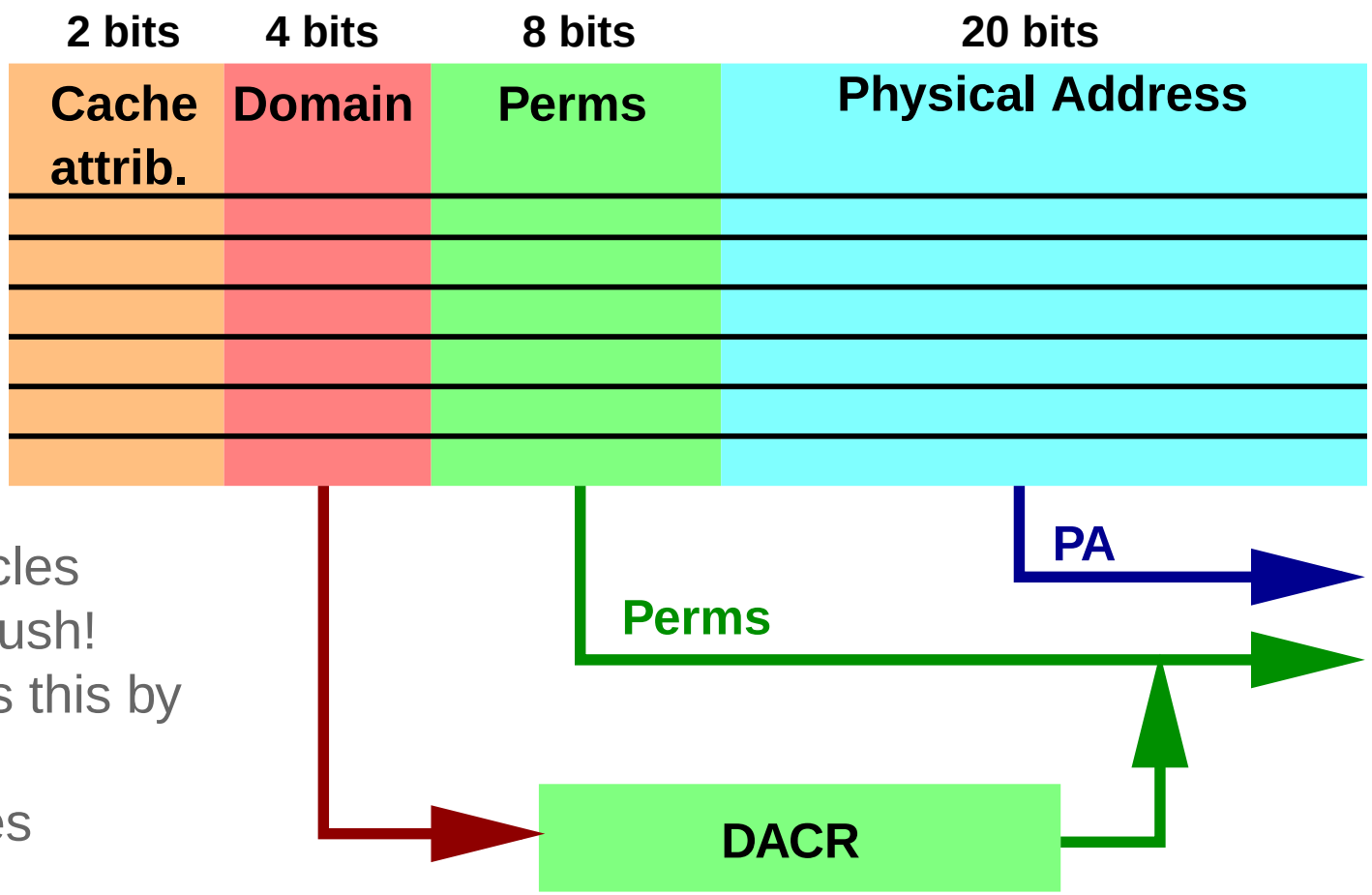
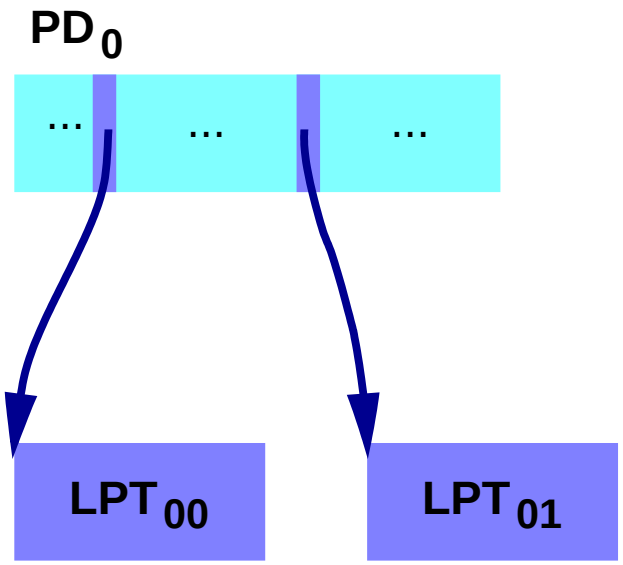


- Better: make use of *domains*
  - ➜ impose additional access restrictions

FAST CONTEXT SWITCH



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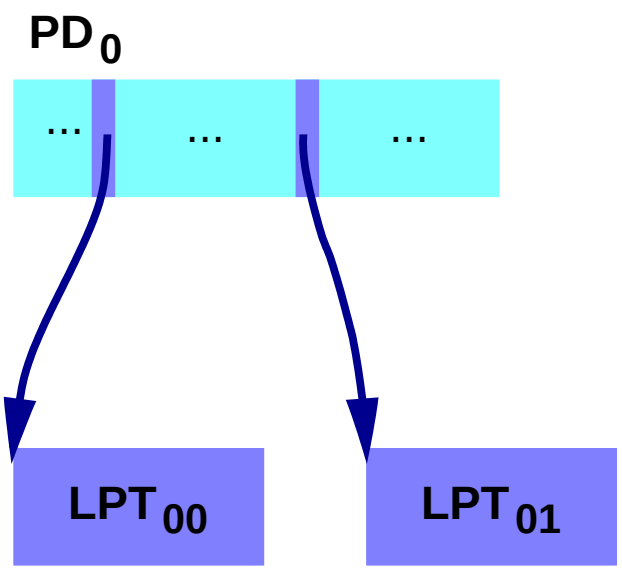

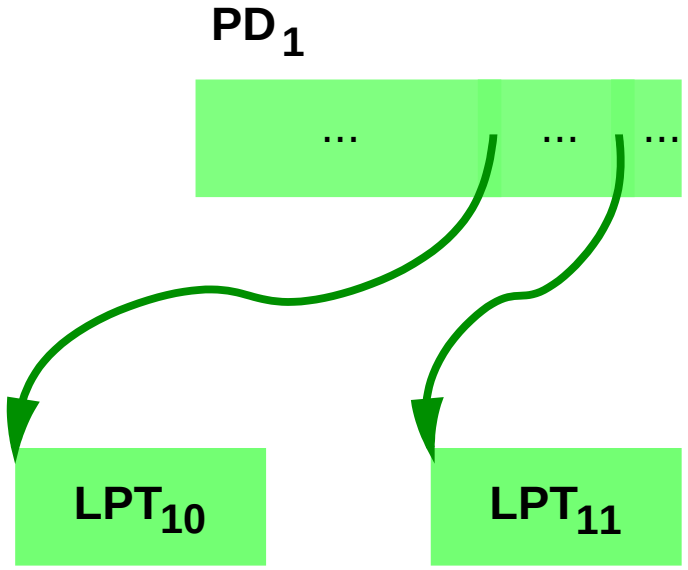

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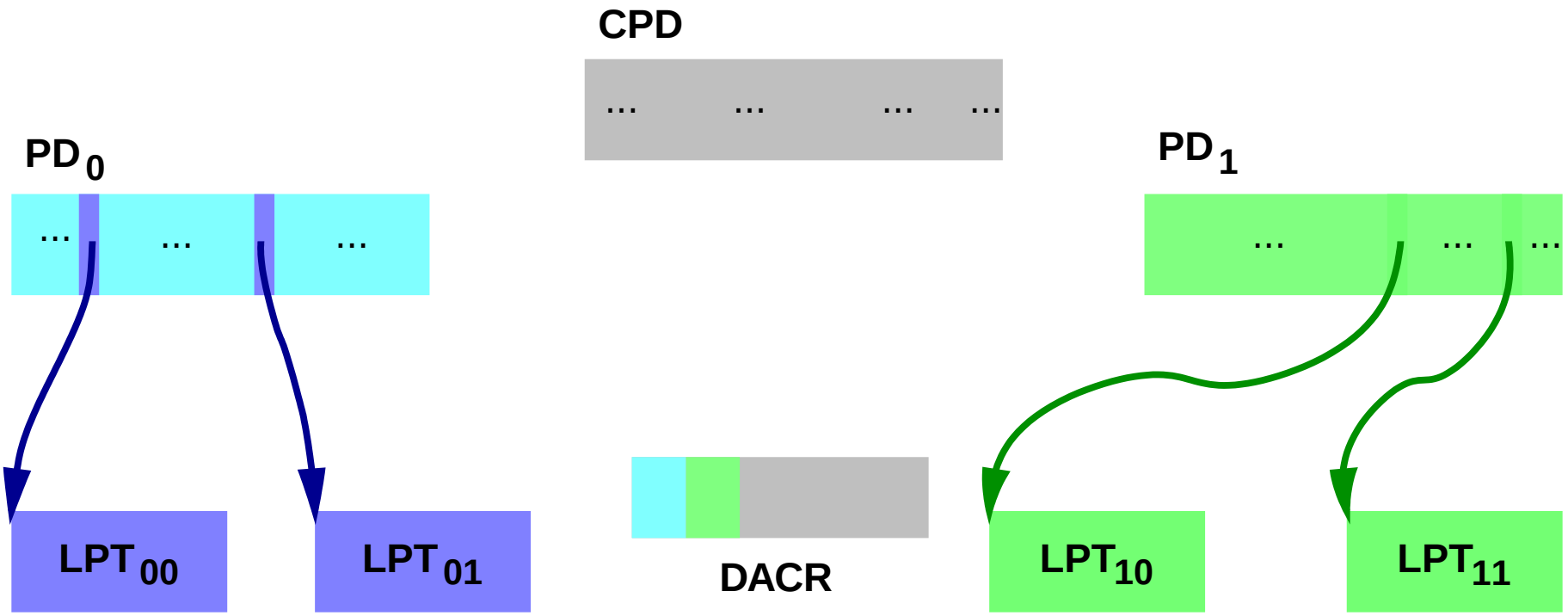

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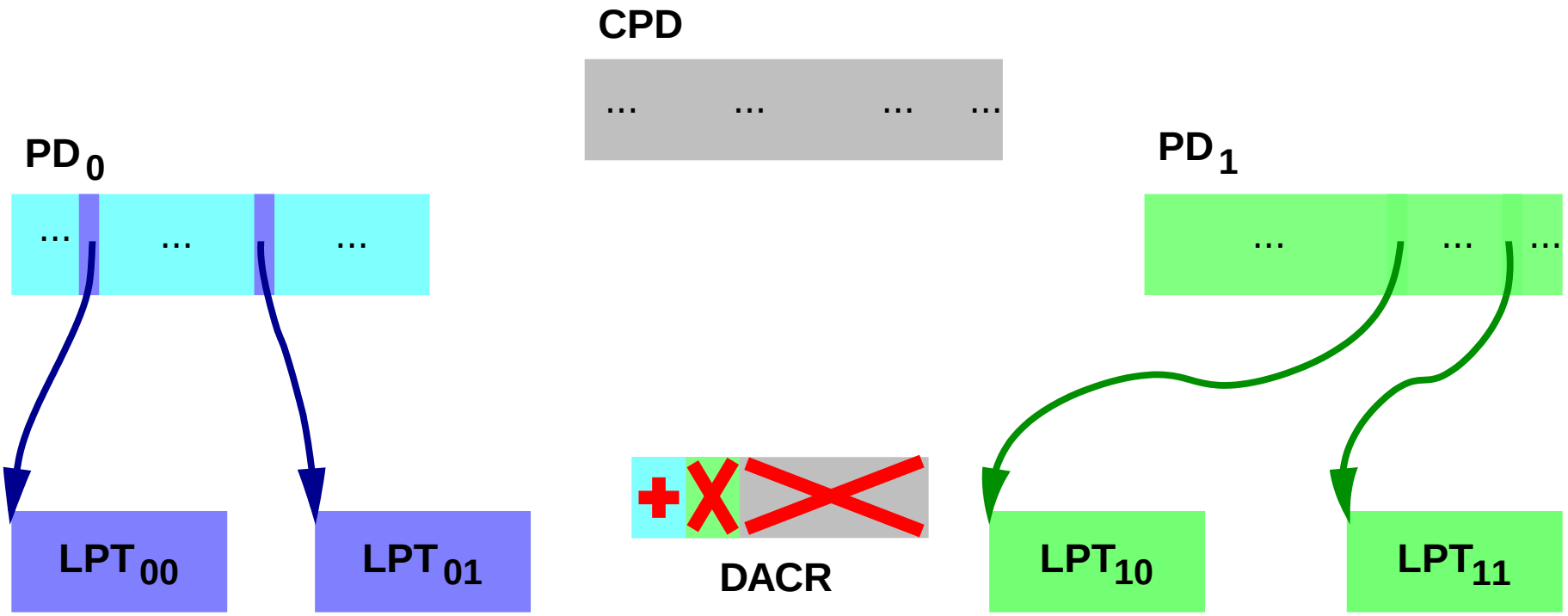

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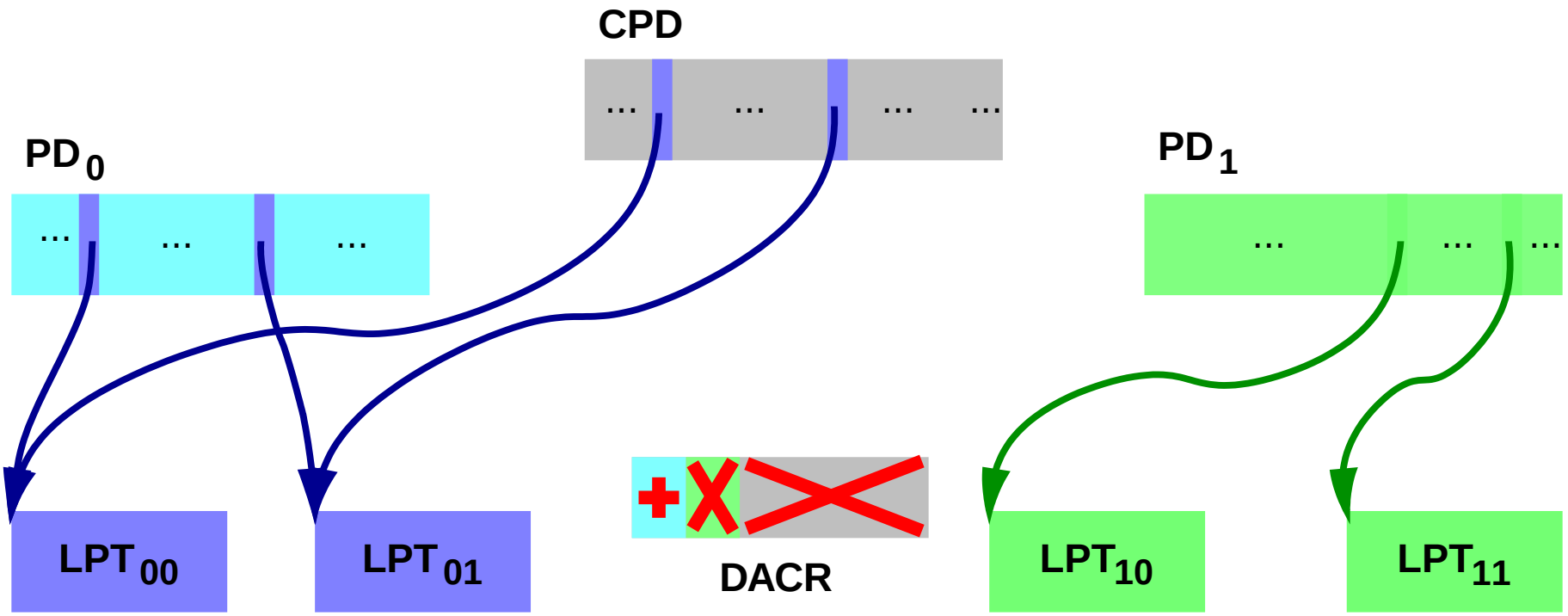

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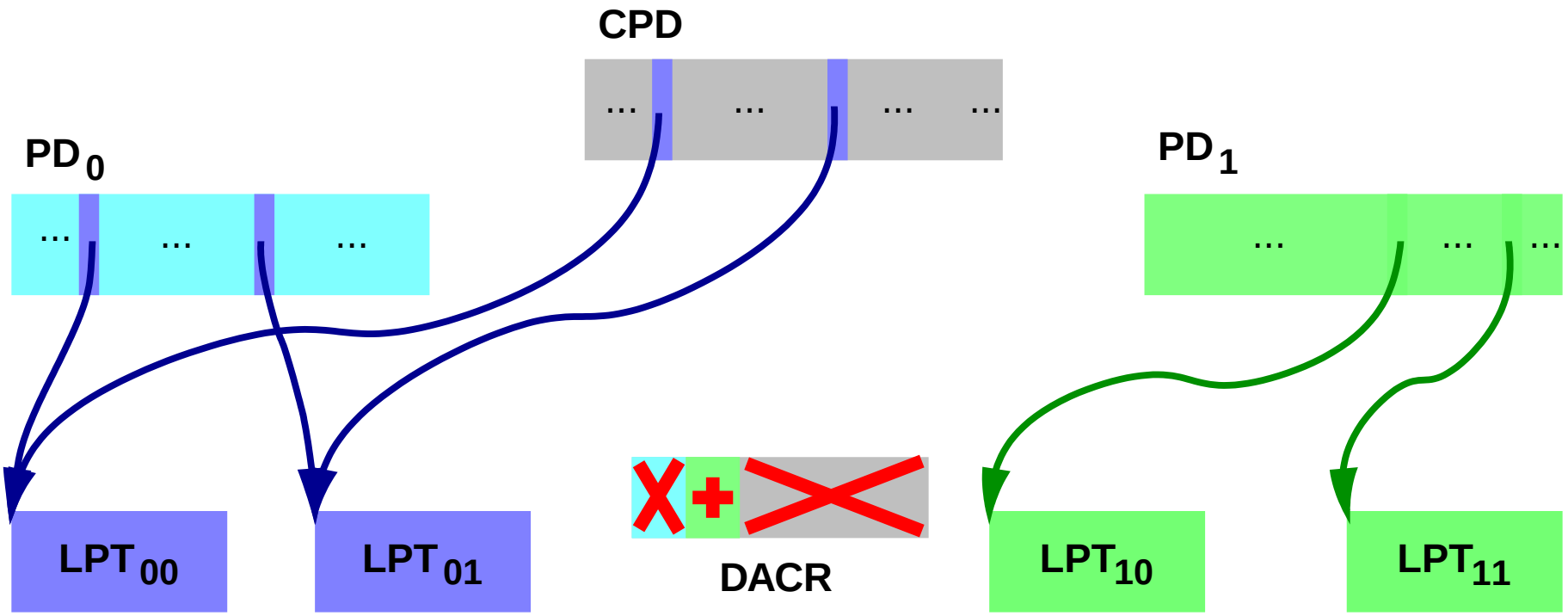

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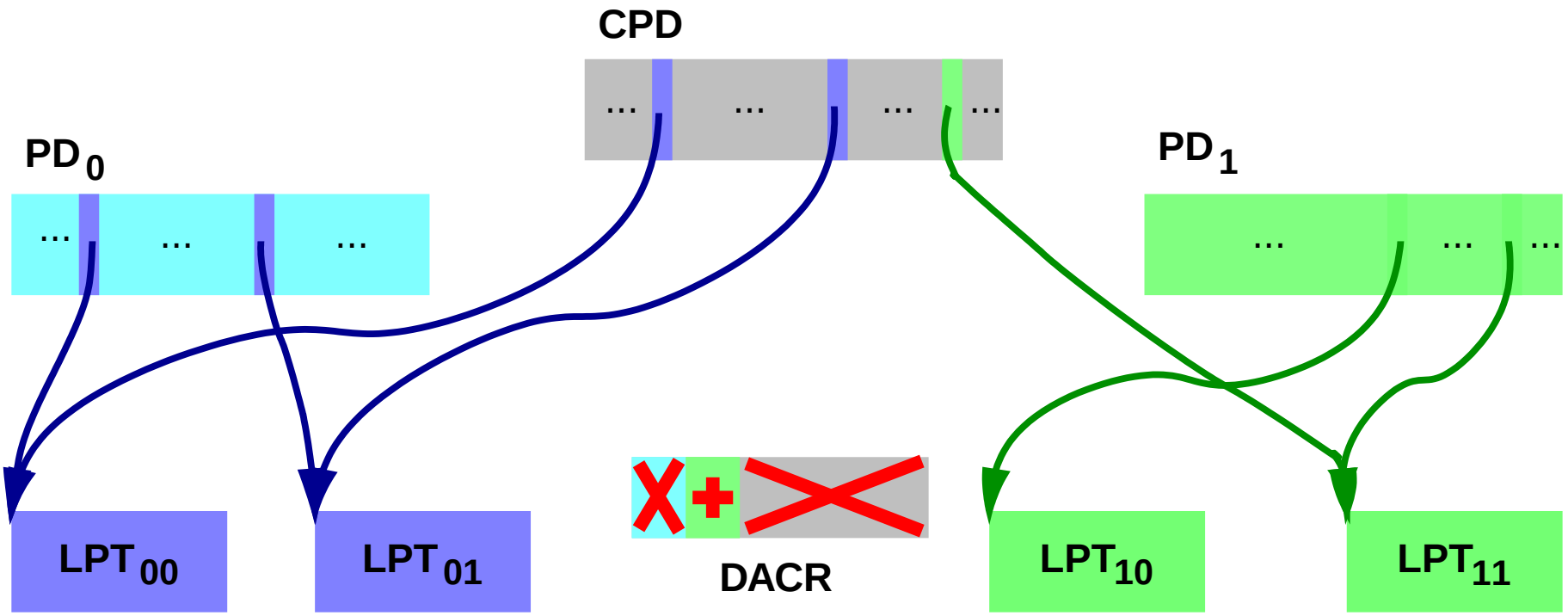

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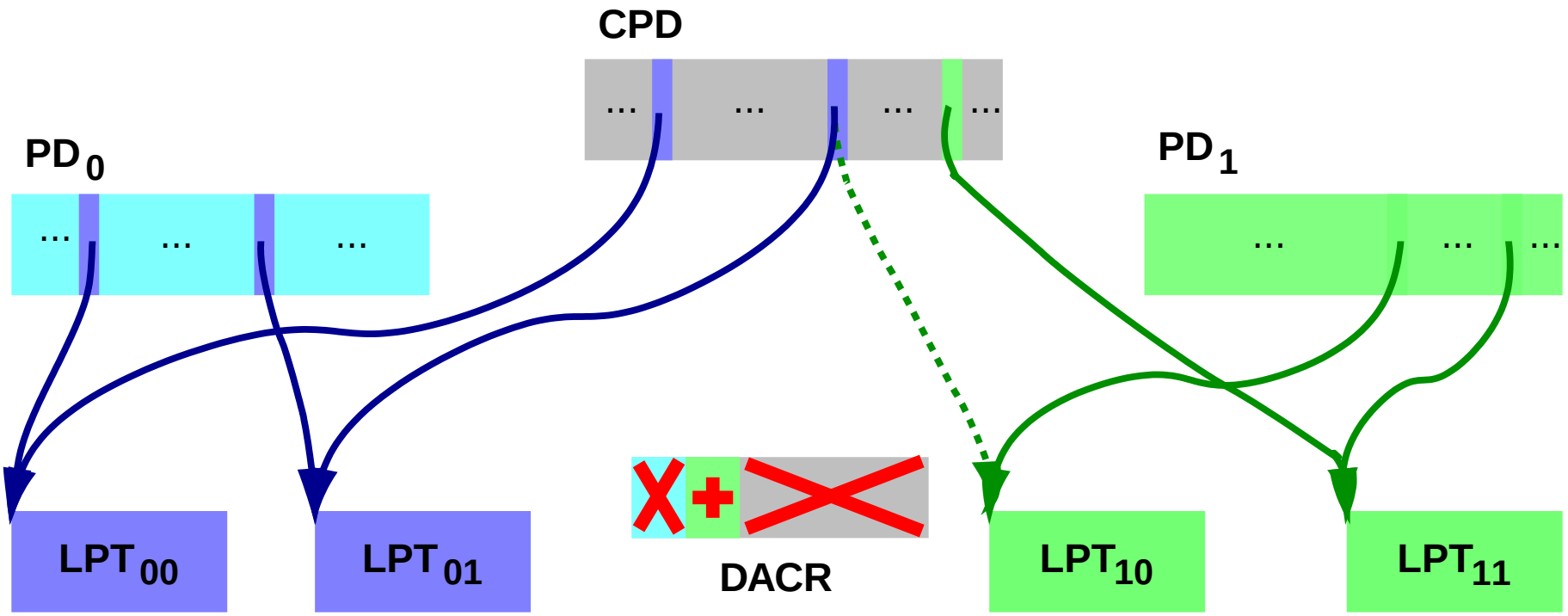

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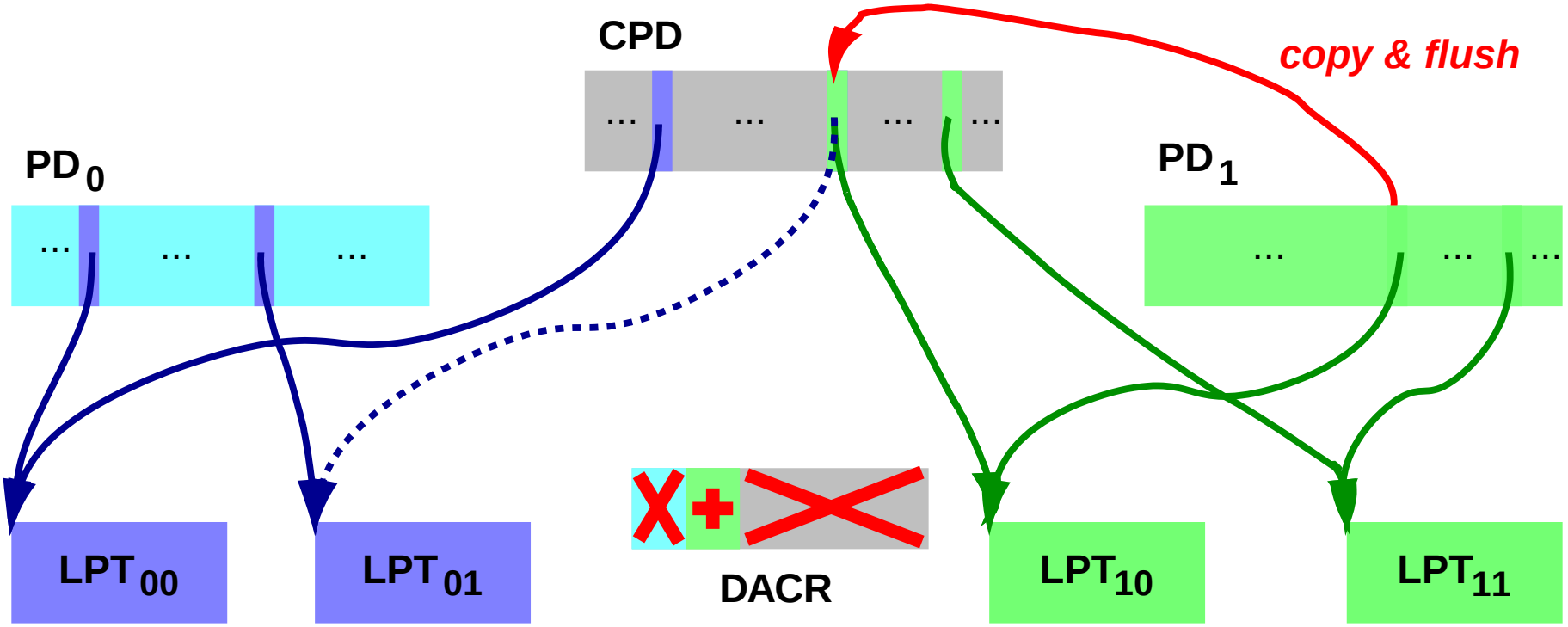

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- ➜ Flush TLB lazily when necessary (on collisions)

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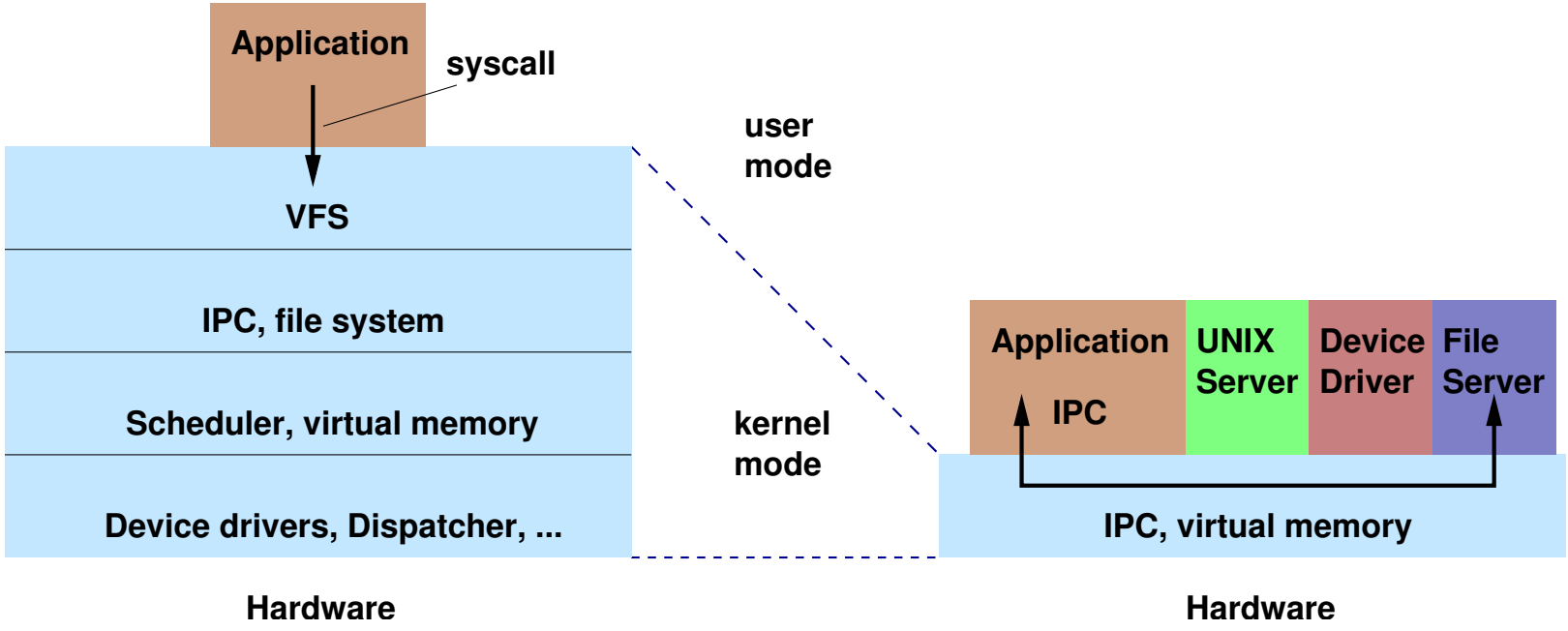
➜ low to medium context-switching rates (dependent on application)

L4Ka::Pistachio: portable implementation of L4 microkernel

➜ high context-switching rates
➜ context-switching costs are extremely critical



LINUX IMPLEMENTATION

- Use PID-relocation for small (< 32MB) address spaces
  - ➜ includes code, stack and initial heap
  - ➜ extra heap allocated via `mmap()` in upper 2GB
  - ➜ shared libraries `mmap()`-ed in upper 2GB
- Large address spaces ($> 32MB$) not relocated
- Use domains for sharing top-level page table
  - ➜ 3 domains reserved by kernel, 13 available for user processes
  - ➜ use domain preemption if running out of domains

Performance: Linux lmbench Results

Benchmark	*original*	*fast*	*improvement*
lmbench hot potato latency [μs]			
`fcntl`	39	25	1.56$\pm$0.4
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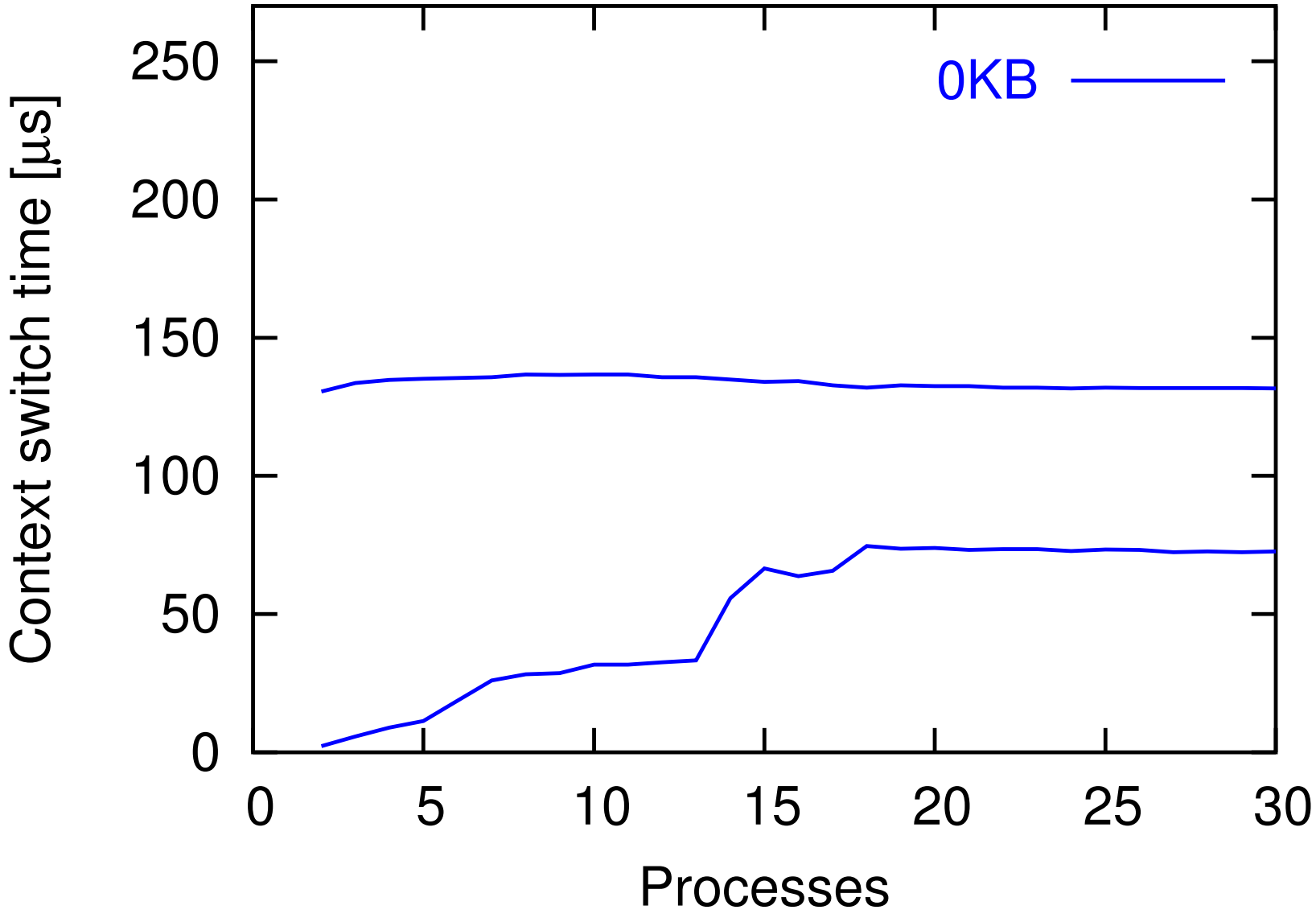
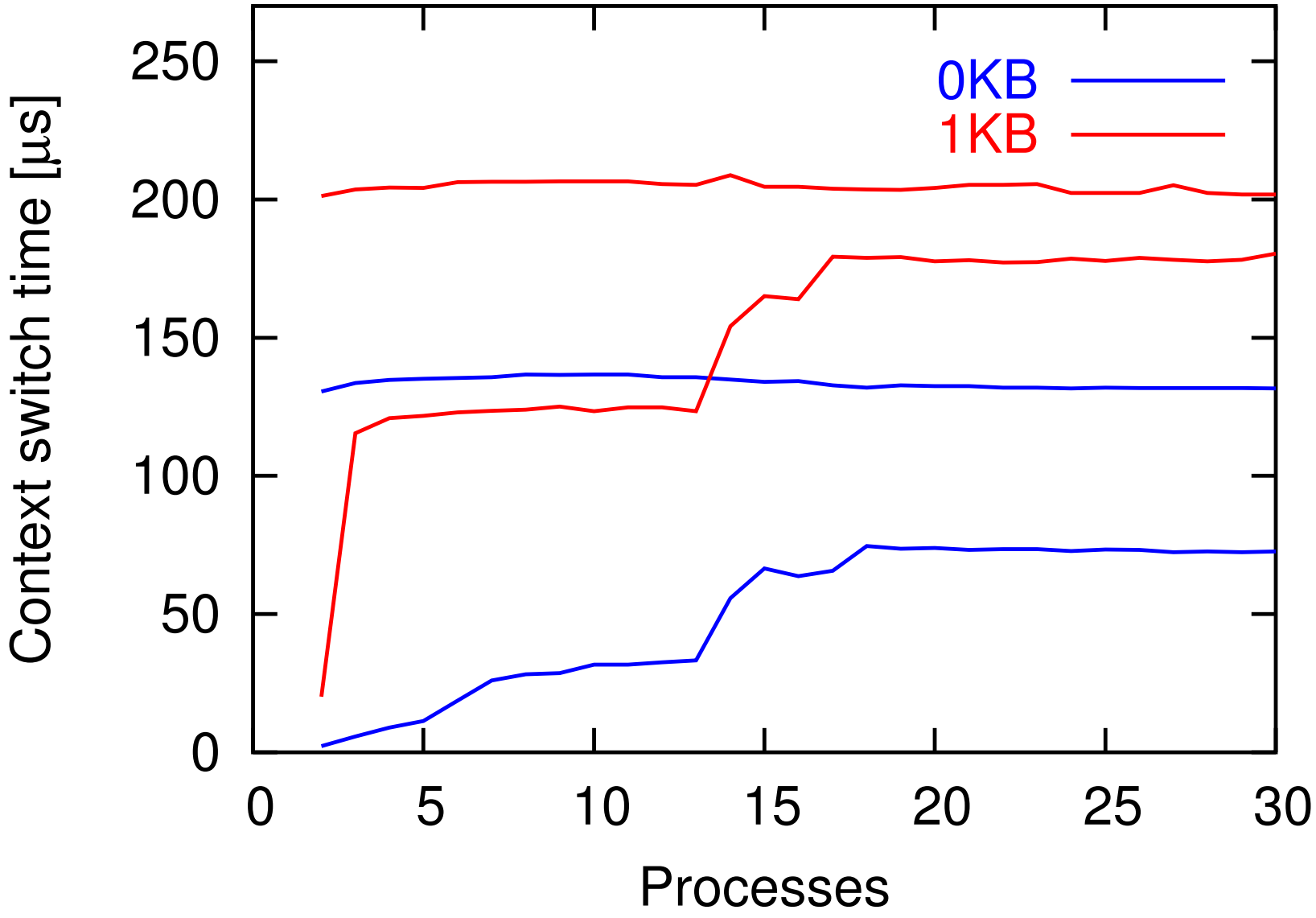
lmbench process creation latency [μs]			
`fork`	4061	3650	1.10±0.00
`exec`	4321	3980	1.08±0.01
`shell`	54533	51726	1.05±0.01

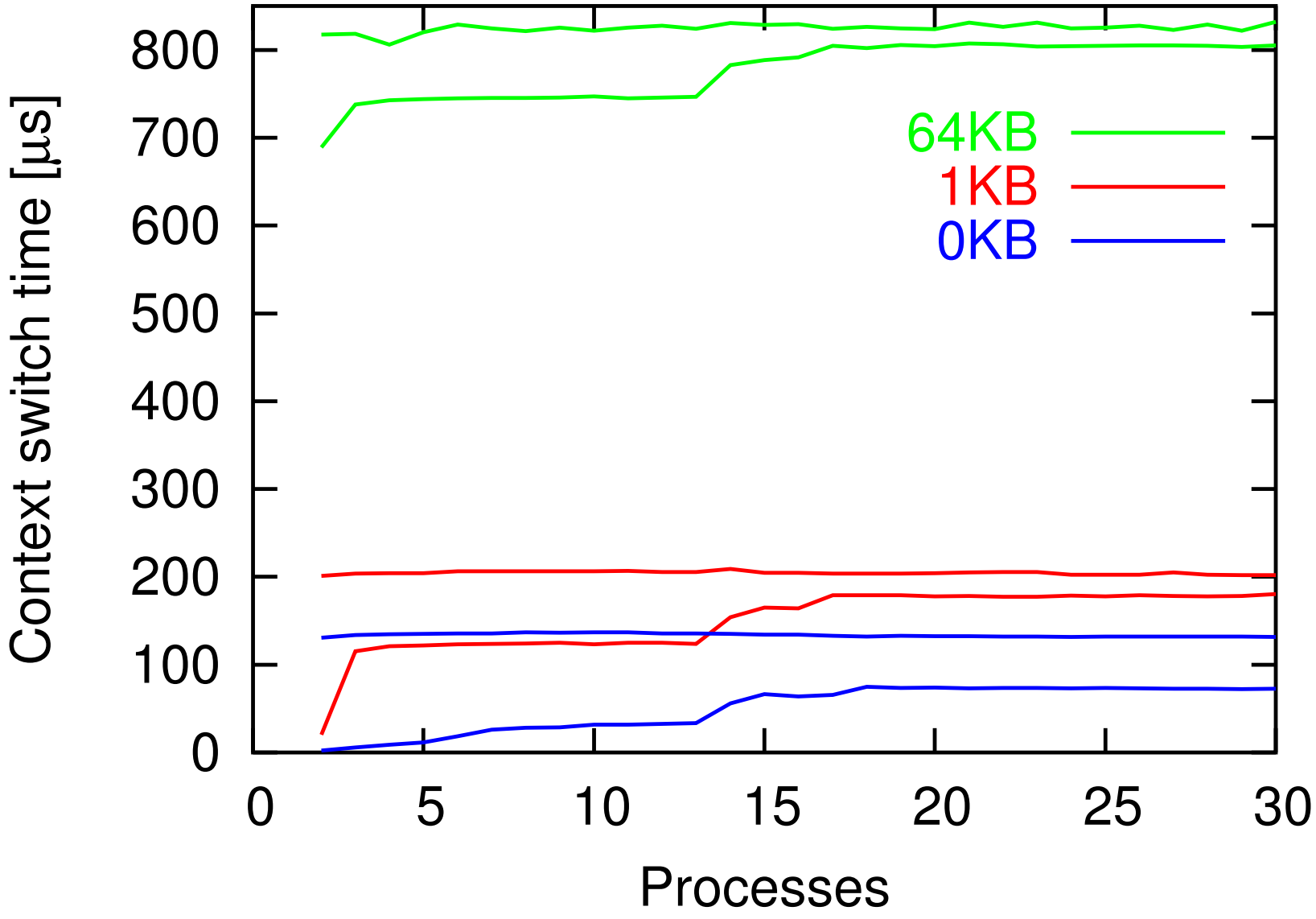
Linux lat_ctx Context Switch Costs



Linux lat_ctx Context Switch Costs



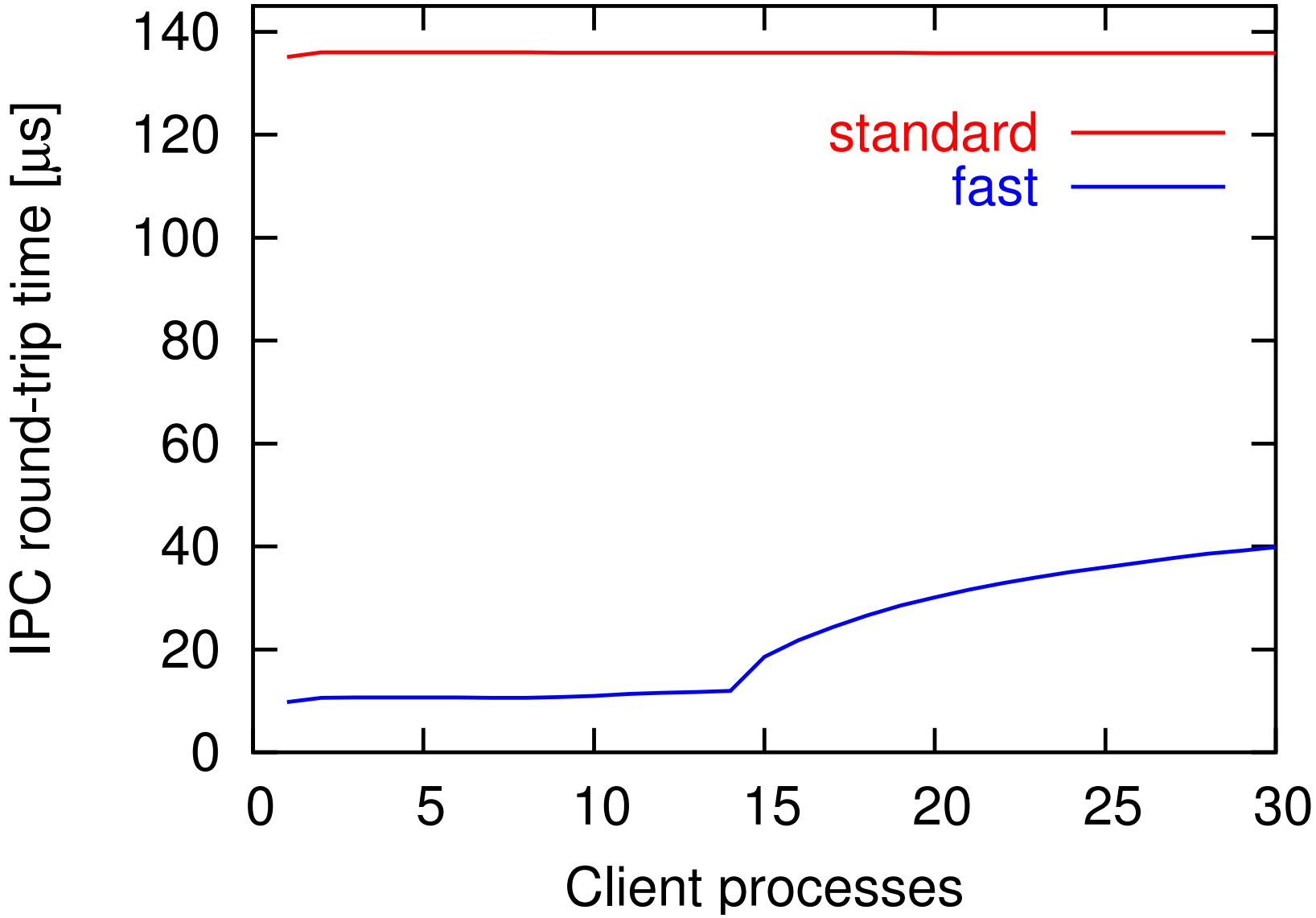
LINUX LAT_CTX CONTEXT SWITCH COSTS



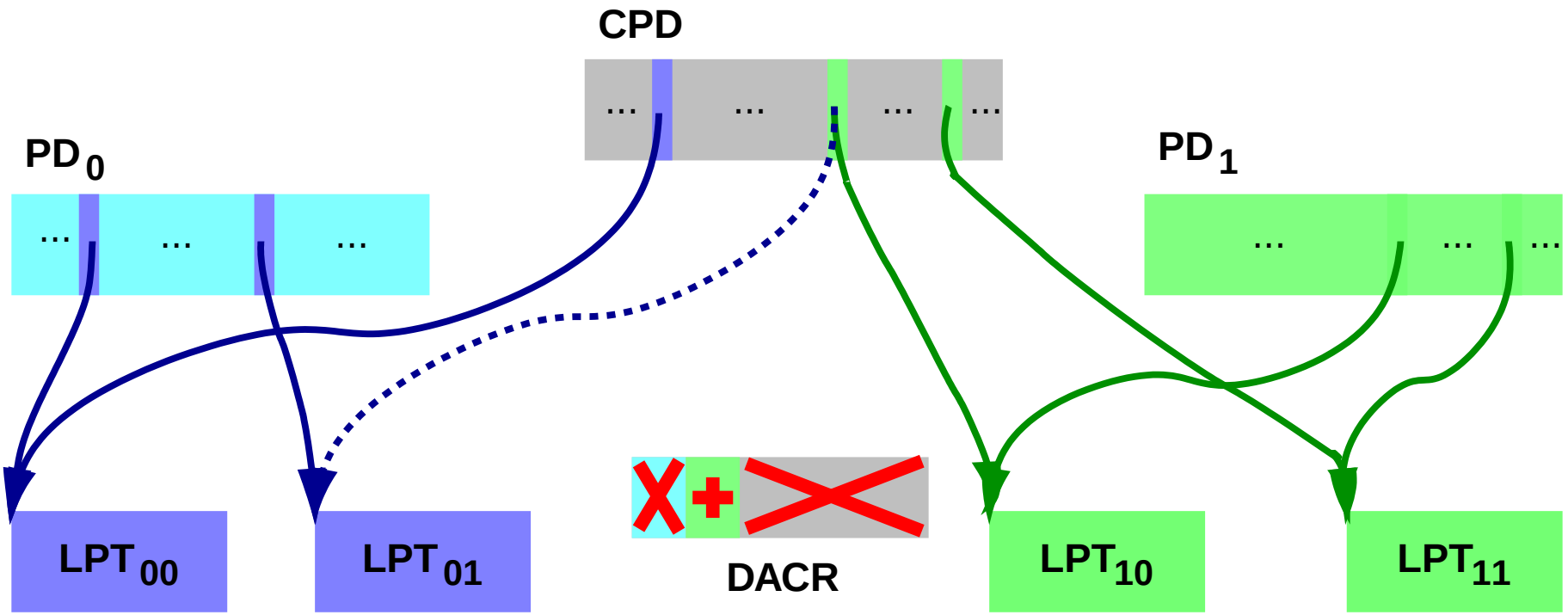
L4 Implementation

- All mappings fully under user control
  - ➜ no specific steps required to avoid collisions
- Use domains for sharing top-level page table
  - ➜ 1 domain reserved by kernel, 15 available for user processes
  - ➜ use domain preemption if running out of domains
  - ➜ keep track of domain use since last flush
    - ➜ if not used since last flush, domain is *clean*
    - ➜ clean domains can be preempted without cache flush

L4 Message-Passing Performance

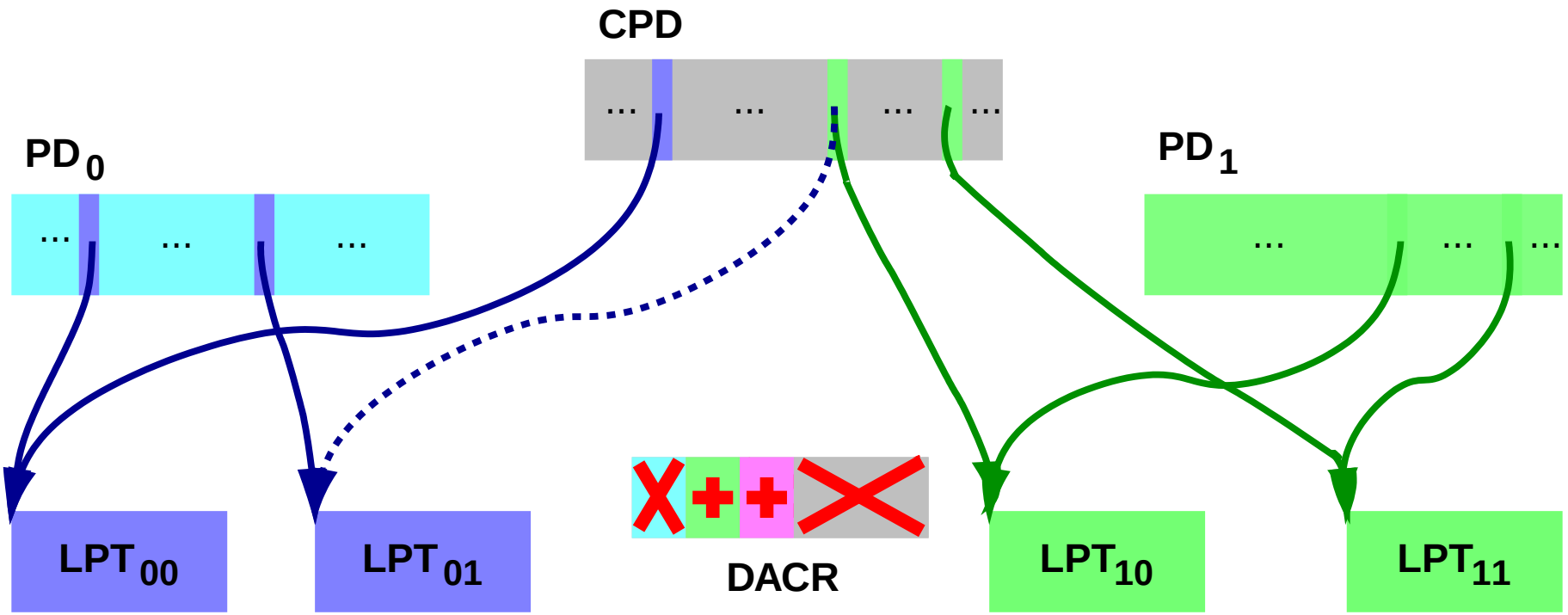


SHARED PAGES



- Shared (rather than conflicting) mappings

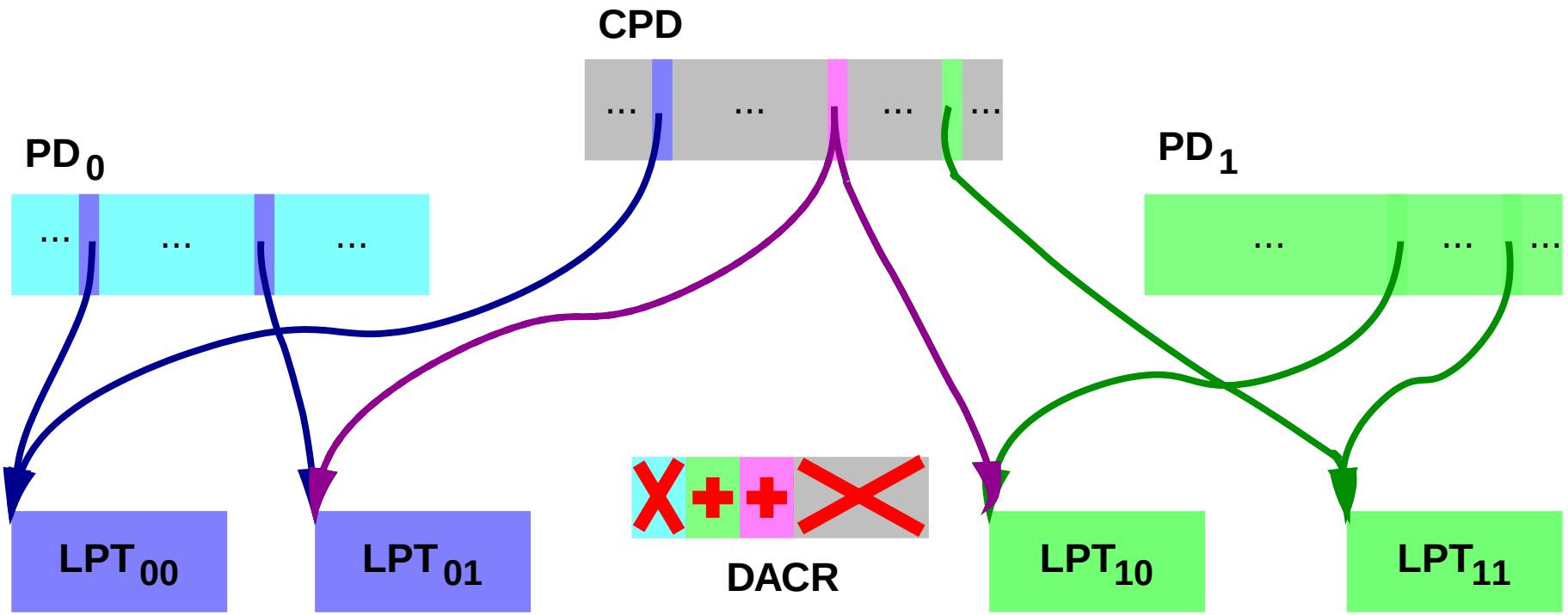
Shared Pages



- Shared (rather than conflicting) mappings:

  ➜ use separate domain for shared mappings

Shared Pages



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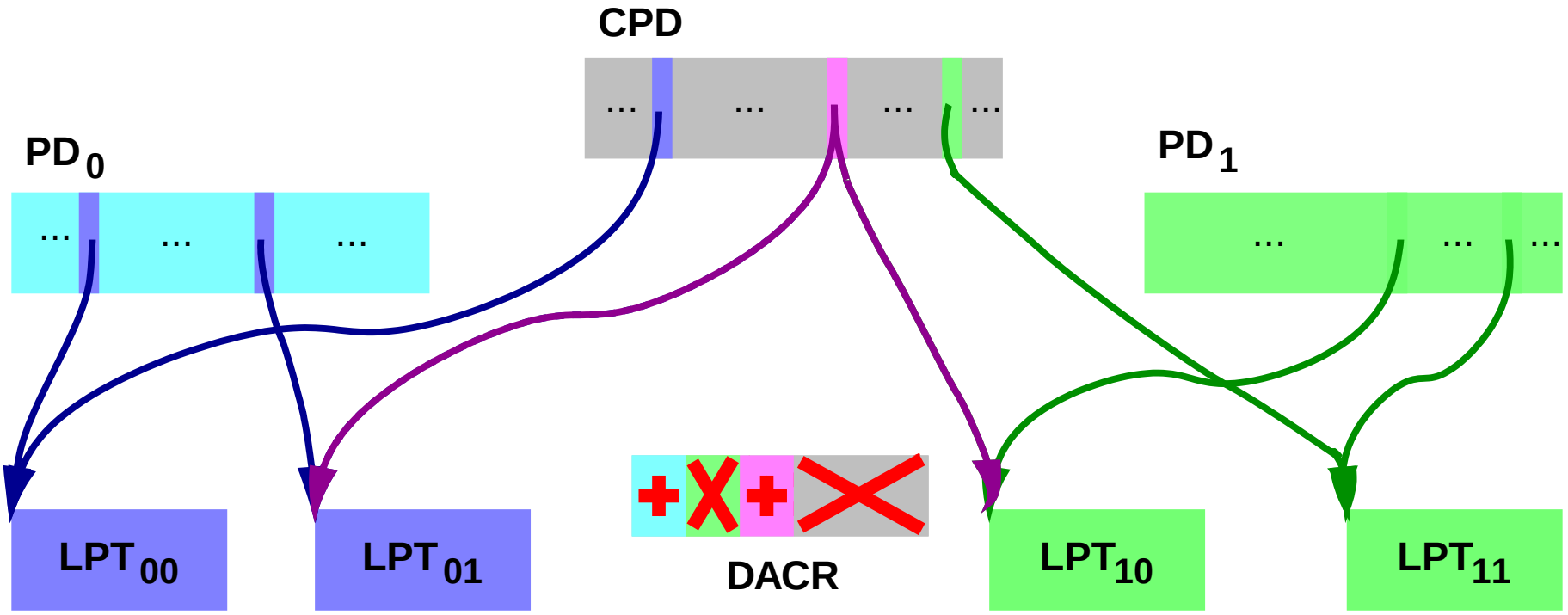
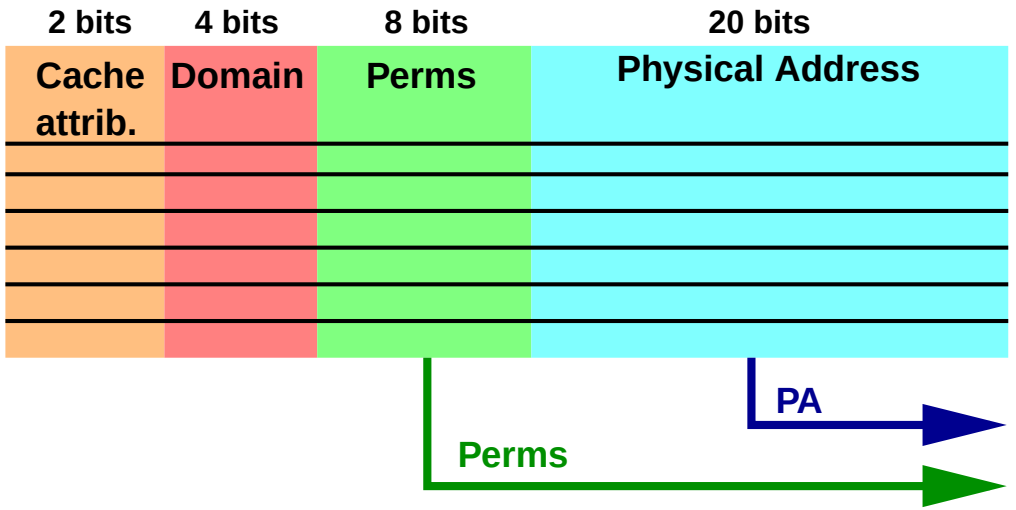


- Shared (rather than conflicting) mappings:
  - ➜ use separate domain for shared mappings
  - ➜ use this to tag shared page table entries
  - ➜ can keep shared mappings valid across context switch

Shared TLB Entries

- Domains are TLB tags



SHARED TLB ENTRIES

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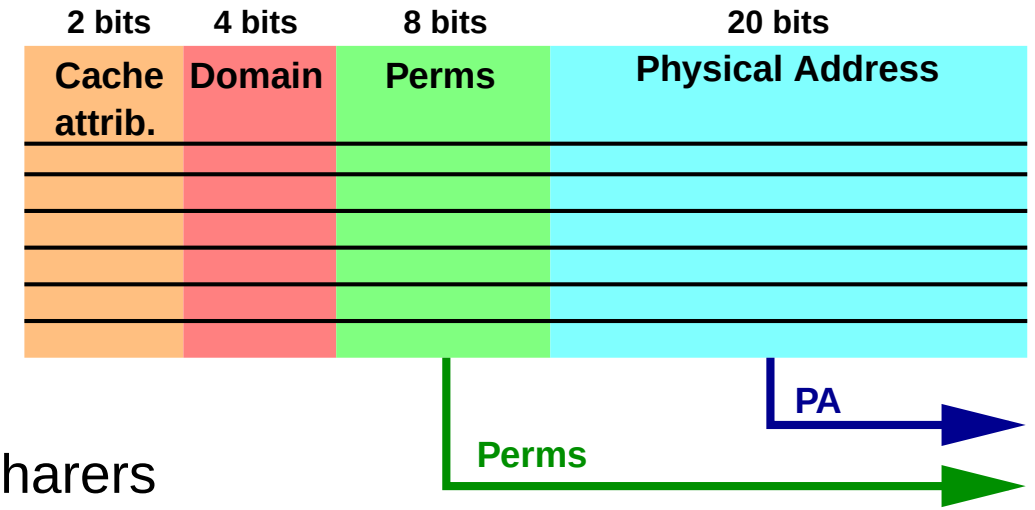
  - ➜ sharing page table entries
    : sharing TLB entries
  - ➜ Single TLB entry for shared page, irrespective of number of sharers



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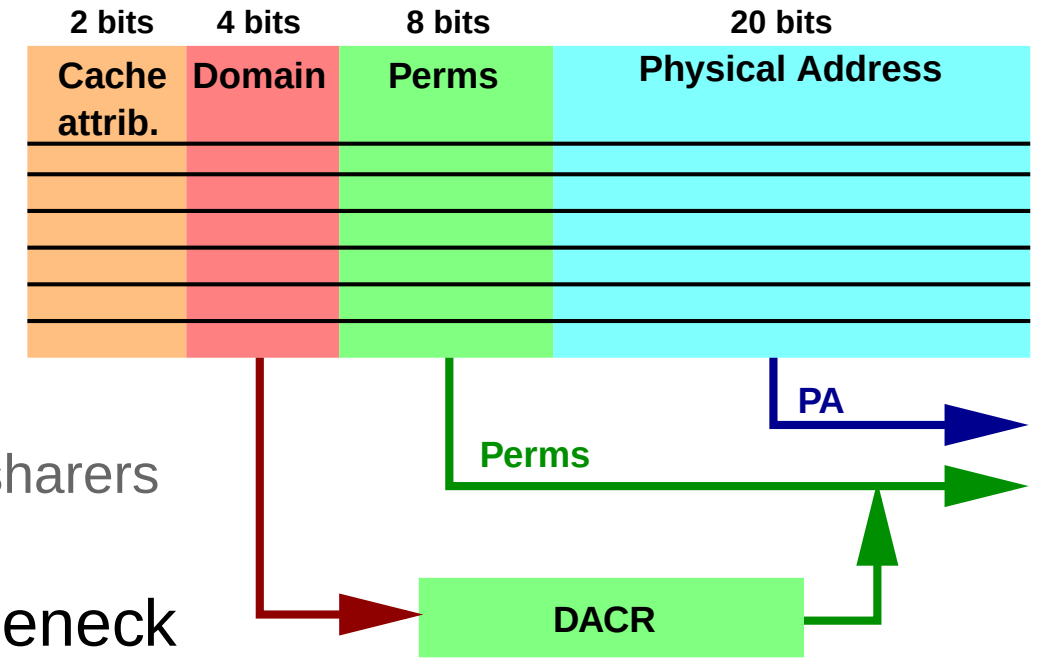

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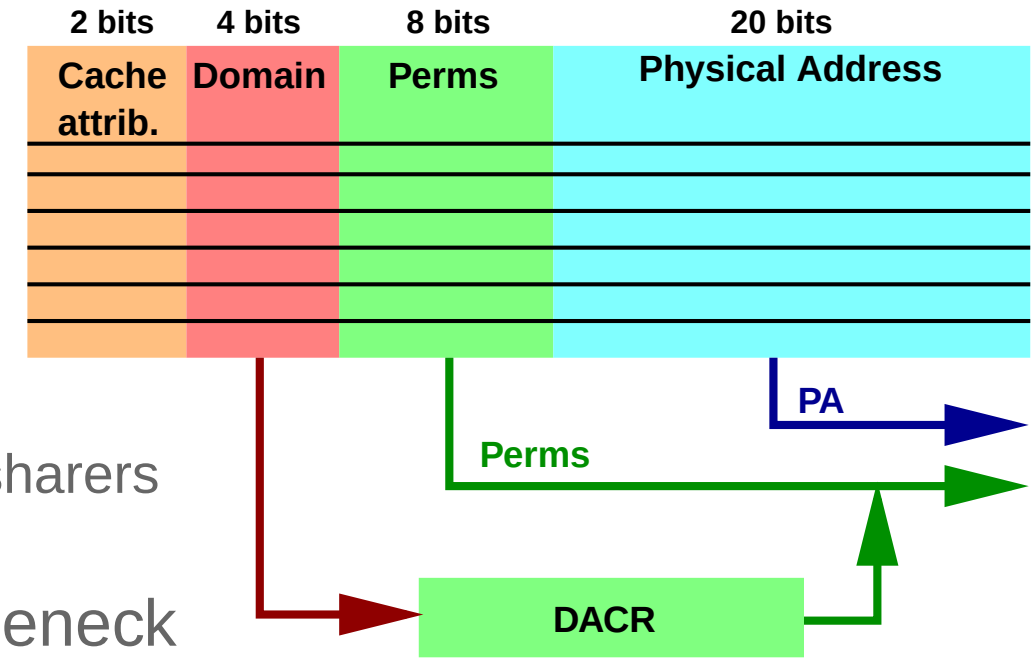
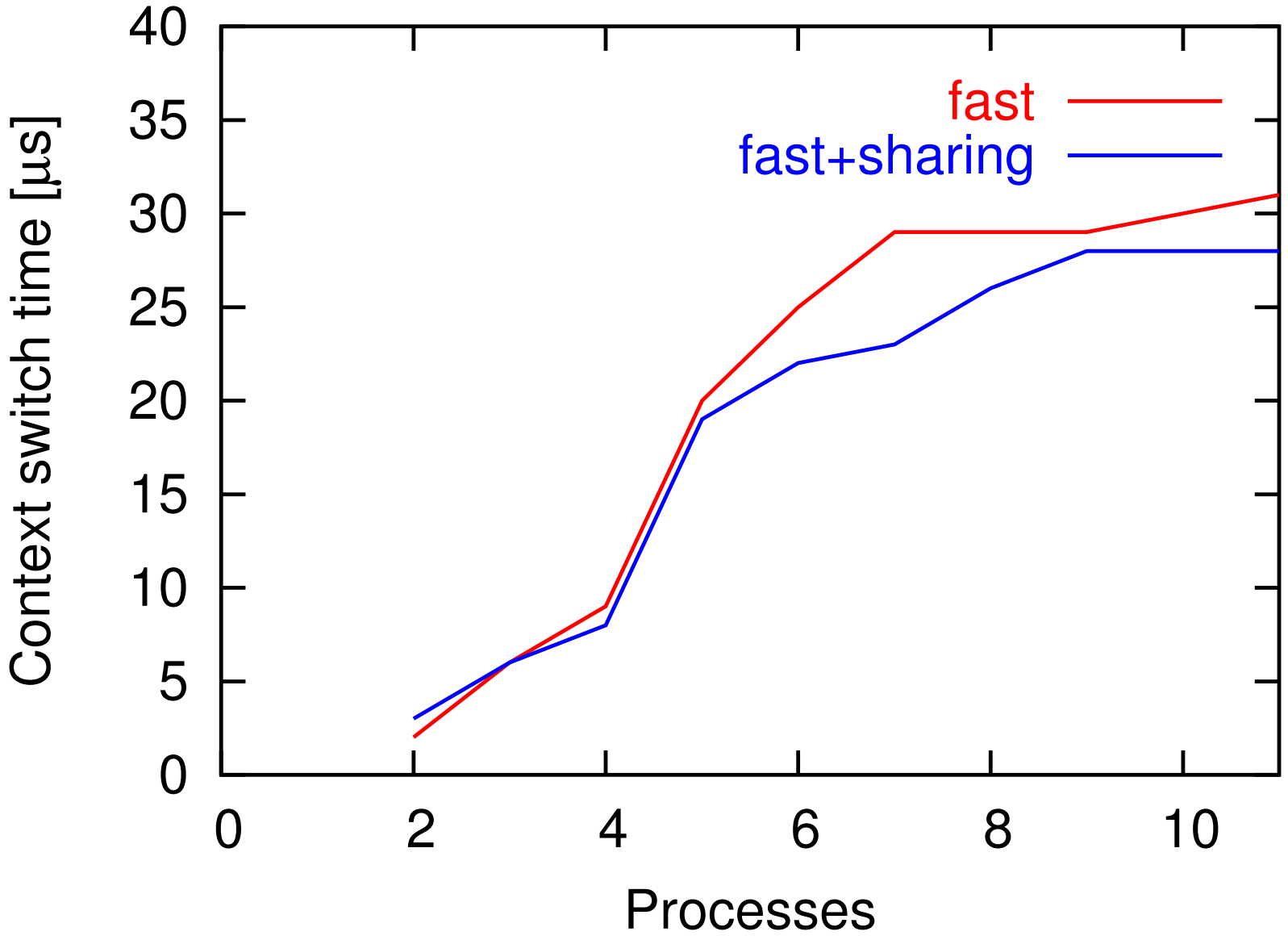
- TLB coverage is a major bottleneck
- TLB entry sharing
  - ➜ reduces the consumption of TLB entries
  - ➜ reduces competition for TLB entries between address spaces
  - ➜ reduces indirect context-switching costs



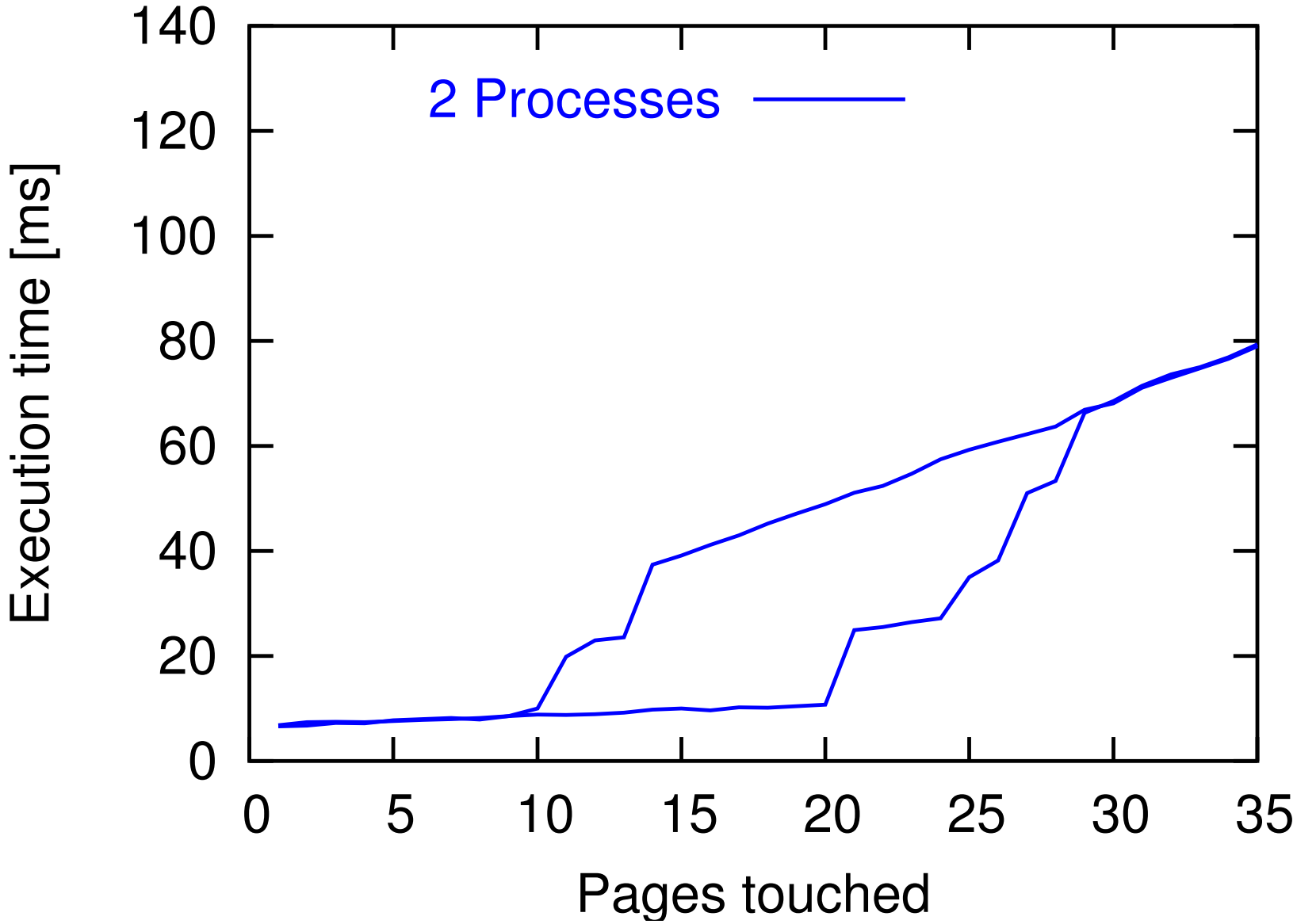
Implementation on Linux

- Transparent to user code
  - ➜ allocate separate domain for each shared region
- For shared libraries use shared domain
  - ➜ text segment mapped to *preferred link address* in upper 2GB
  - ➜ private linking as fall-back if address already in use
  - ➜ data segment relocated to process-specific region (lower 32MB)
- Some tricks required to make this work
  - ➜ see paper for details

LINUX LAT_CTX CONTEXT SWITCH COSTS



Taking it to the Extreme



"Extreme" benchmark maximises context switching and sharing

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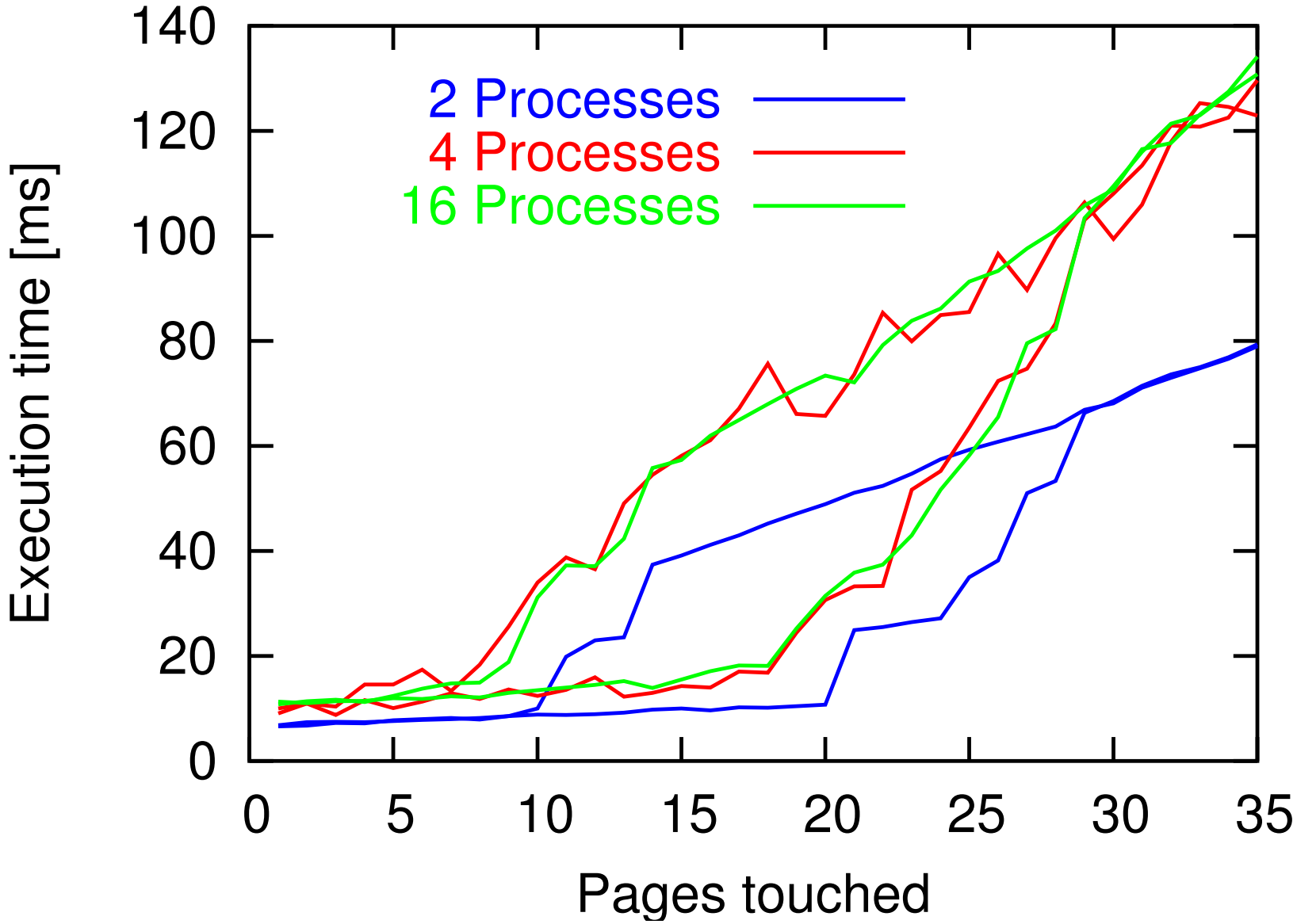

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CONCLUSIONS

- Fast context switching using domains is a clear winner
  - ➜ orders of magnitude reduction in context-switching overhead on SA-1100
  - ➜ never seen a case where “fast” kernel was slower than vanilla
  - ➜ similar improvements expected on XScale

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  - ➜ however, SGI has benchmarks which significantly benefit from TLB sharing

REFERENCES

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