Microkernels
In a Bit More Depth

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COMP9242 2005/S2 Week 5

MOTIVATION

- Early operating systems had very little structure.
- A strictly layered approach was promoted by [Dijkstra 1968].
- Later OS (more or less) followed that approach (e.g., Unix).
- Such systems are known as *monolithic kernels*

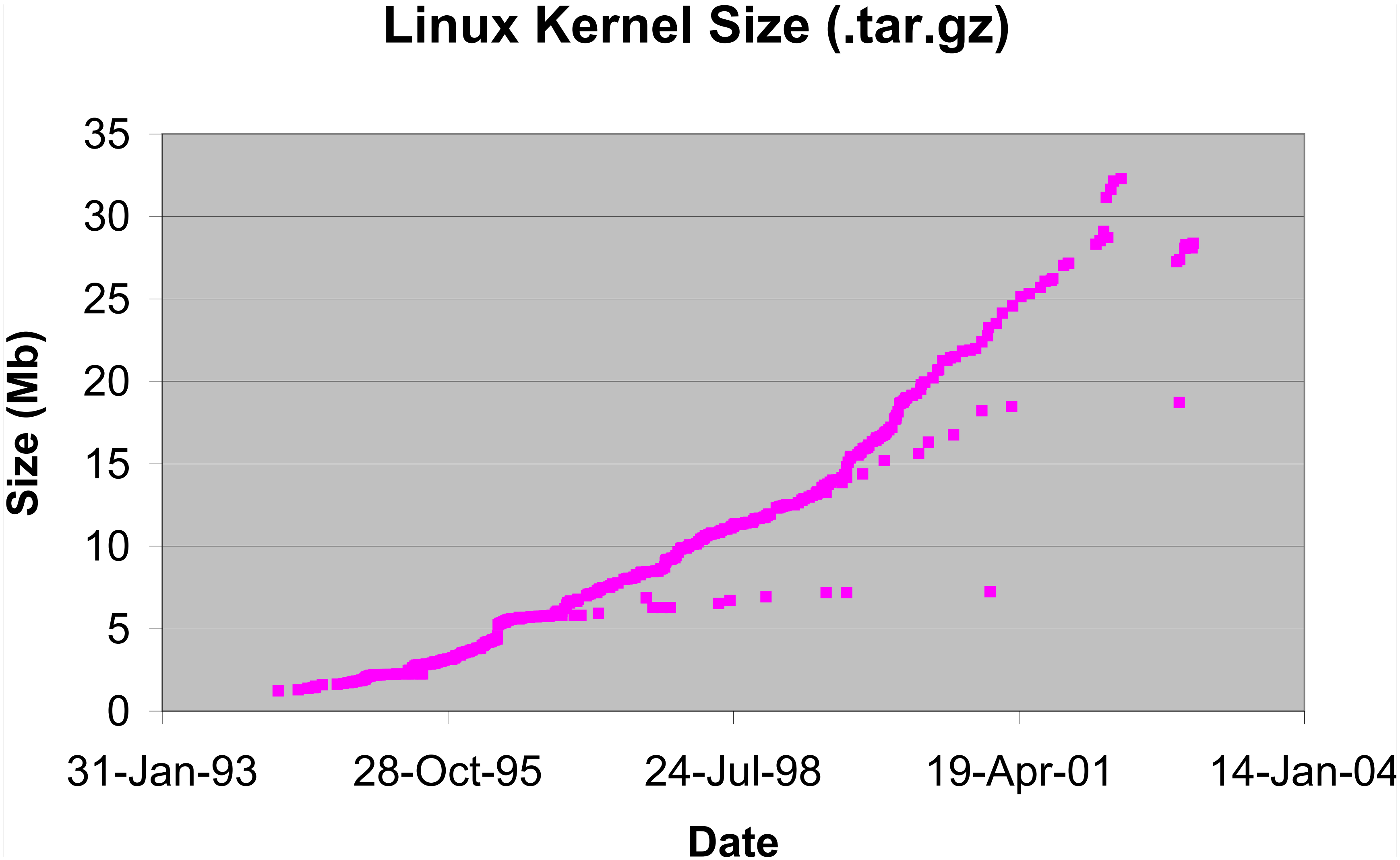
ADVANTAGES OF MONOLITHIC KERNELS

- Kernel has access to everything:
  - ➜ all optimisations possible
  - ➜ all techniques/mechanisms/concepts implementable
- Kernel can be extended by adding more code, e.g. for:
  - ➜ new services
  - ➜ support for new hardare

PROBLEMS WITH LAYERED APPROACH

- Widening range of services and applications
  $\Rightarrow$ OS bigger, more complex, slower, more error prone.
- Need to support same OS on different hardware.
- Like to support various OS environments.
- Distribution
  $\Rightarrow$ impossible to provide all services from same (local) kernel.

EVOLUTION OF THE LINUX KERNEL



Linux 2.4.18: 2.7M LoC

APPROACHES TO TACKLING COMPLEXITY

- Classical software-engineering approach: modularity
  - ➜ (relatively) small, mostly self-contained components
  - ➜ well-defined interfaces between them
  - ➜ enforcement of interfaces
  - ➜ containment of faults to few modules

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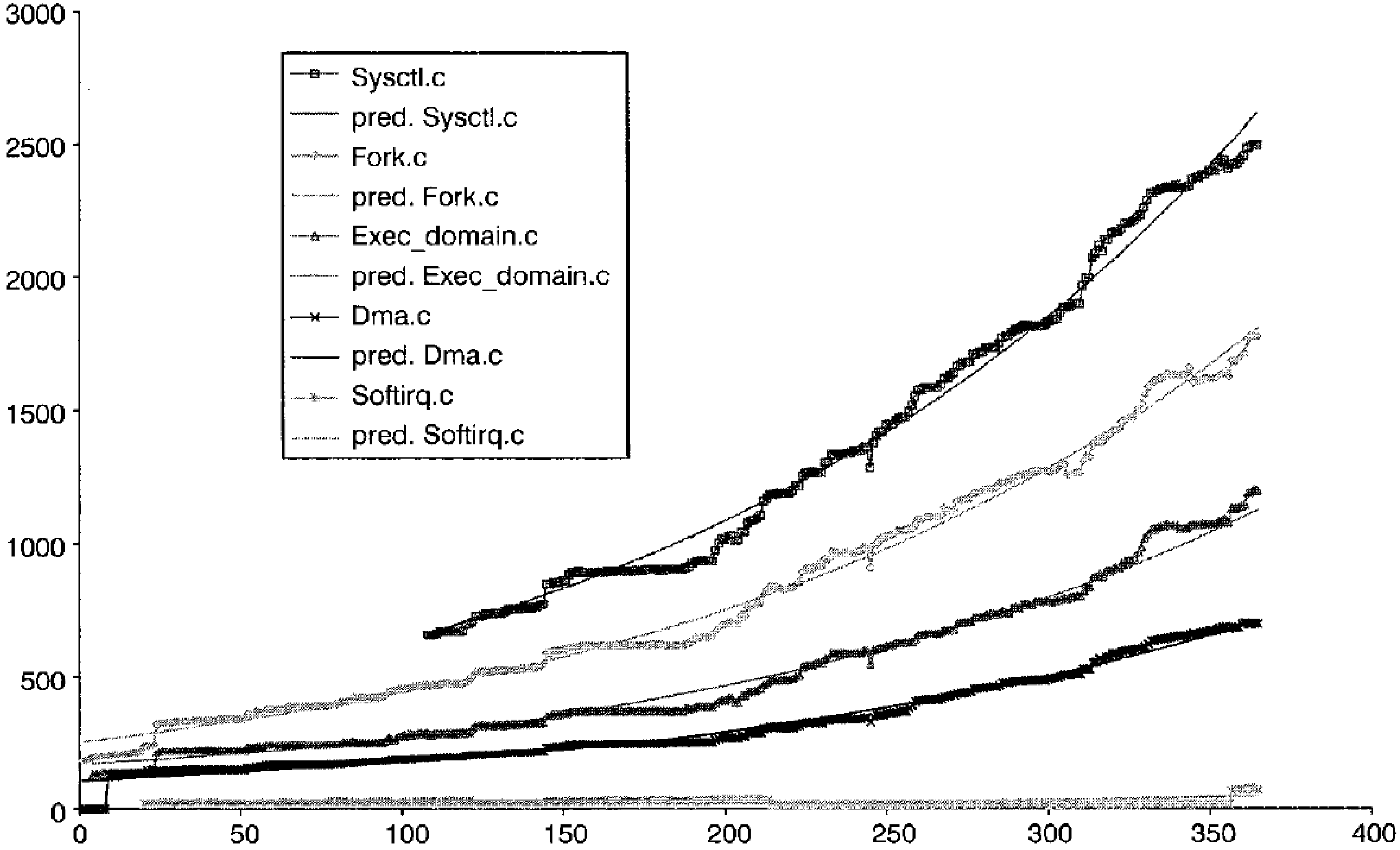
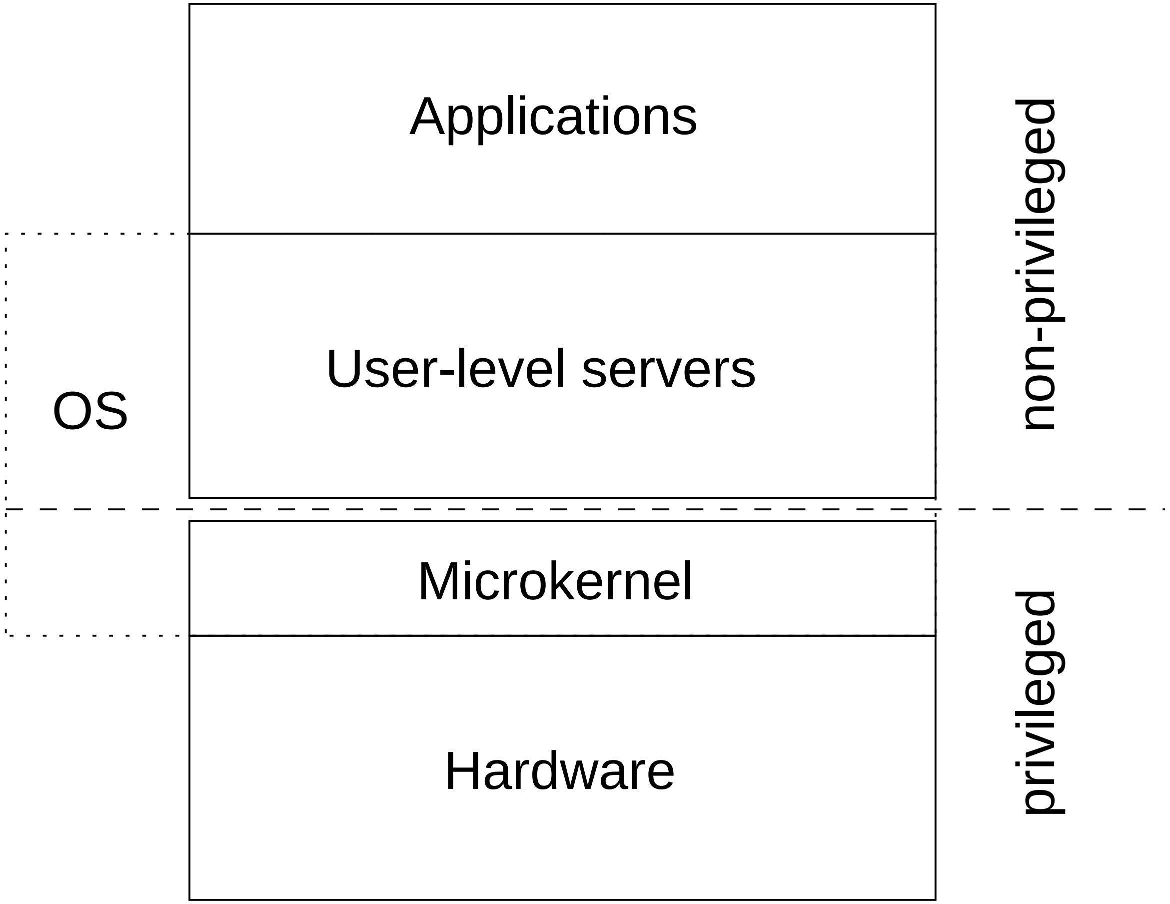
  - ➜ containment of faults to few modules
- Doesn’t work with monolithic kernels:
  - ➜ all kernel code executes in privileged mode
    - ➜ faults aren’t contained
    - ➜ interfaces cannot be enforced
    - ➜ performance takes priority over structure

EVOLUTION OF THE LINUX KERNEL — PART 2



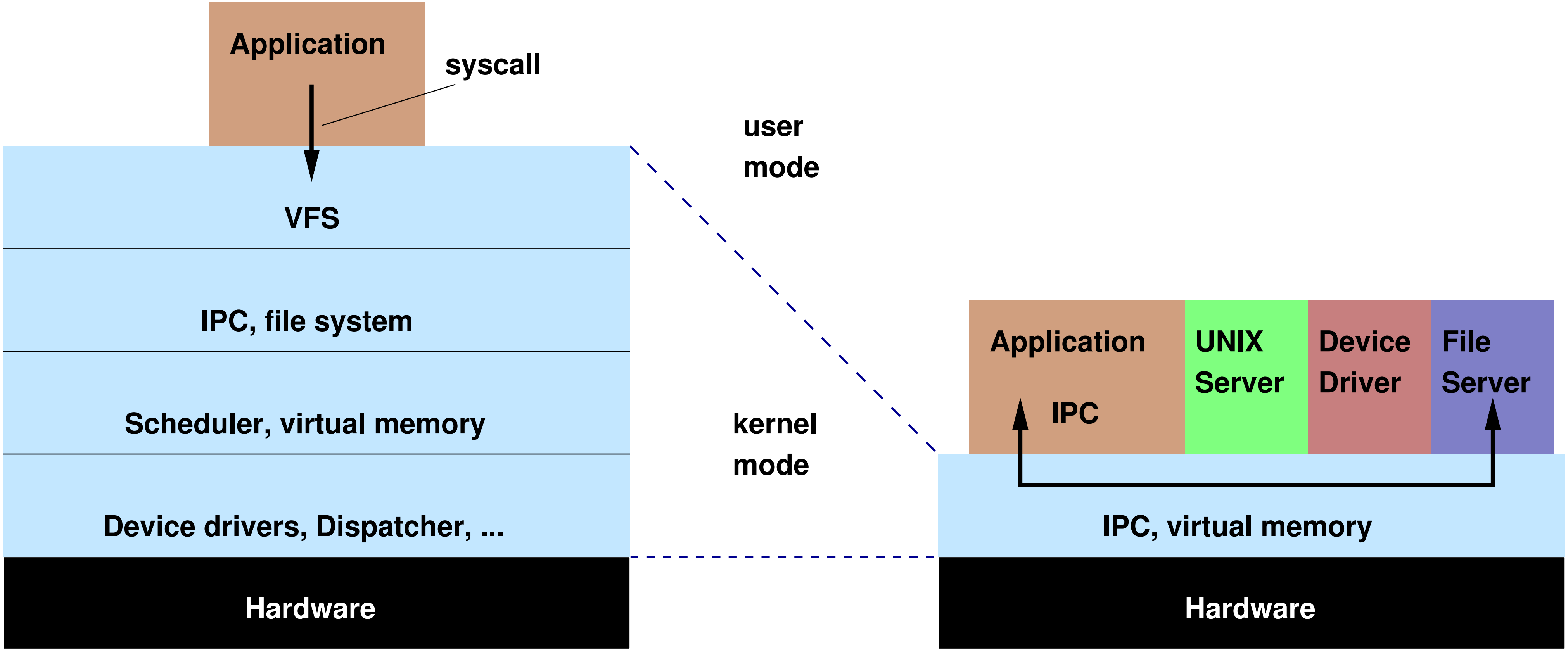
Dependencies between kernel modules by global variables ("common coupling") as a function of version number [SJW$^+$02]: *Exponential growth!*

MICROKERNEL IDEA: BREAK UP THE OS



Based on the ideas of Brinch Hansen's "Nucleus" [BH70]

MONOLITHIC VS. MICROKERNEL OS STRUCTURE



MICROKERNEL OS

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  - ⋆ contains code which *must* run in supervisor mode;
  - ⋆ isolates hardware dependence from higher levels;
  - ⋆ is small and fast
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- User-level servers:
  - ⋆ are hardware independent/portable,
  - ⋆ provide “OS environment”/”OS personality” (maybe several),
  - ⋆ may be invoked:
    - ➜ from **application** (via message-passing IPC)
    - ➜ from **kernel** (upcalls);

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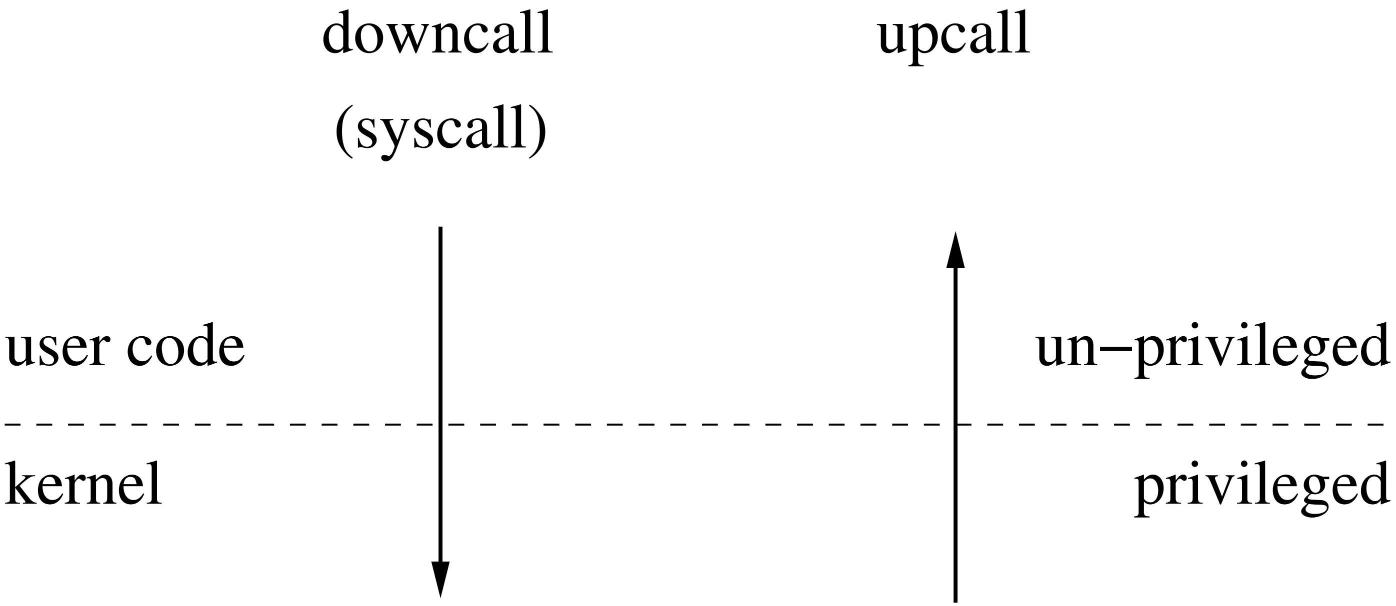
  - ⋆ implement *policies* [BH70].

DOWNCALL VS. UPCALL



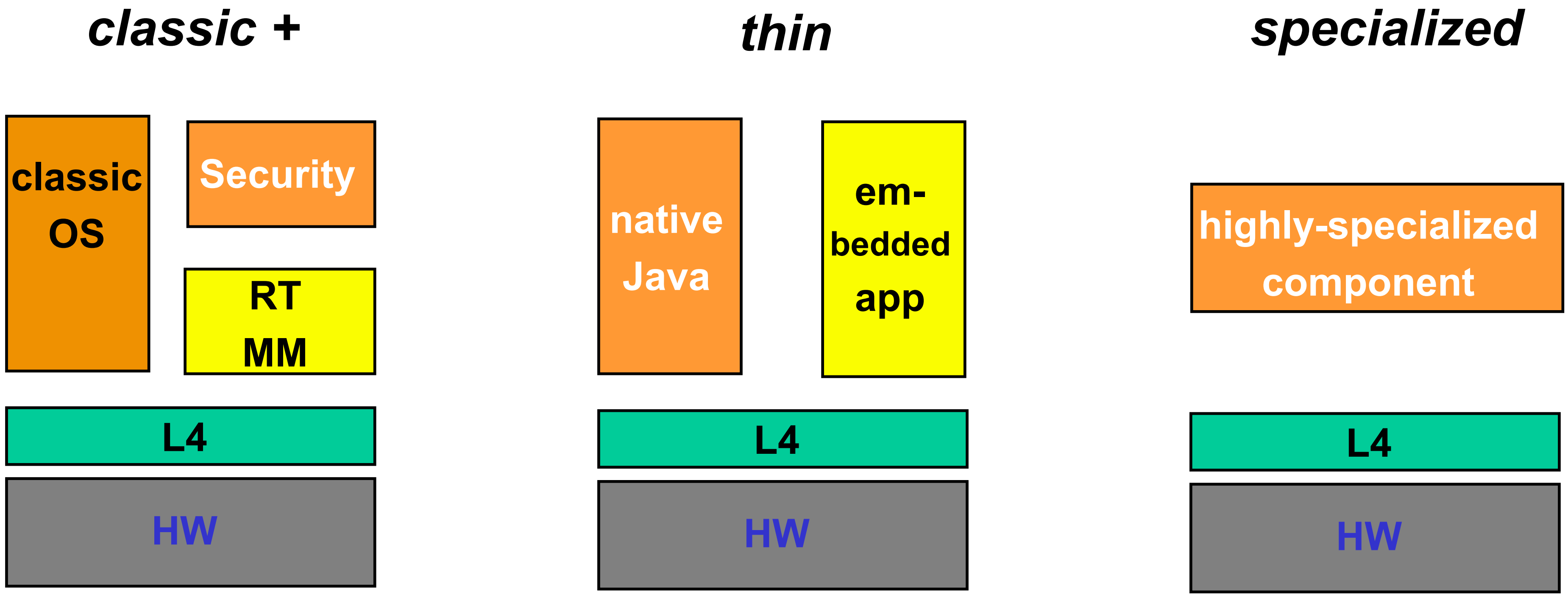
unprivileged code
enters kernel mode

implemented via trap

privileged code
enters user mode

implemented via IPC

MICROKERNEL-BASED SYSTEMS



EARLY EXAMPLE: HYDRA

- Separation of mechanism from policy
  - ➜ e.g. protection vs. security
- No hierarchical layering of kernel.
- Protection, even within OS.
  - ➜ Uses (segregated) *capabilities*.
- Objects, encapsuation, units of protection.
- Unique object *name*, no ownership.
- Object persistence based on reference counting [WCC$^+$74].

HYDRA ...

- Can be considered the first *object-oriented* OS;
- Has been called the first *microkernel* OS (by people who ignored Brinch Hansen)
- Has had enormous influence on later operating systems research;
- Was never widely used even at CMU because of
  - ➜ poor performance,
  - ➜ lack of a complete environment.

POPULAR EXAMPLE: MACH

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Coined term *microkernel*.

BASIC FEATURES OF MACH KERNEL

- Task and thread management
- Interprocess communication (asynchronous message-passing)
- Memory object management
- System call redirection
- Device support
- Multicomputer support

MACH TASKS AND THREADS

- Task consists of one or more threads
- Task provides *address space* and other environment
- Thread is active entity (basic unit of CPU utilisation)
- Threads have own stacks, are kernel scheduled
- Threads may run in parallel on multiprocessor
- “Privileged user-state program” may be used to control scheduling
- Task created from “blueprint” with empty or inherited address space
- Activated by creating a thread in it

MACH IPC: PORTS

- Addressing based on ports:
  - ➜ port is a mailbox, allocated/destroyed via a system call
  - ➜ has a fixed-size message queue associated with it
  - ➜ is protected by (segregated) capabilities
  - ➜ has exactly *one receiver*, but possibly *many senders*
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- Kernel detects ports without senders or receiver
- Processes may have many ports (UNIX server has 2000!)
- Ports can be grouped into *port sets*
  - ➜ Allows listening to many ports (like `select()`)

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- Send blocks if queue is full
  - ➜ except with send-once cap (used for server replies)

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  - ➜ kernel marshalls capabilities in messages
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  - ⋆ optional send capability to reply port
    - ➜ for use by receiver to send reply
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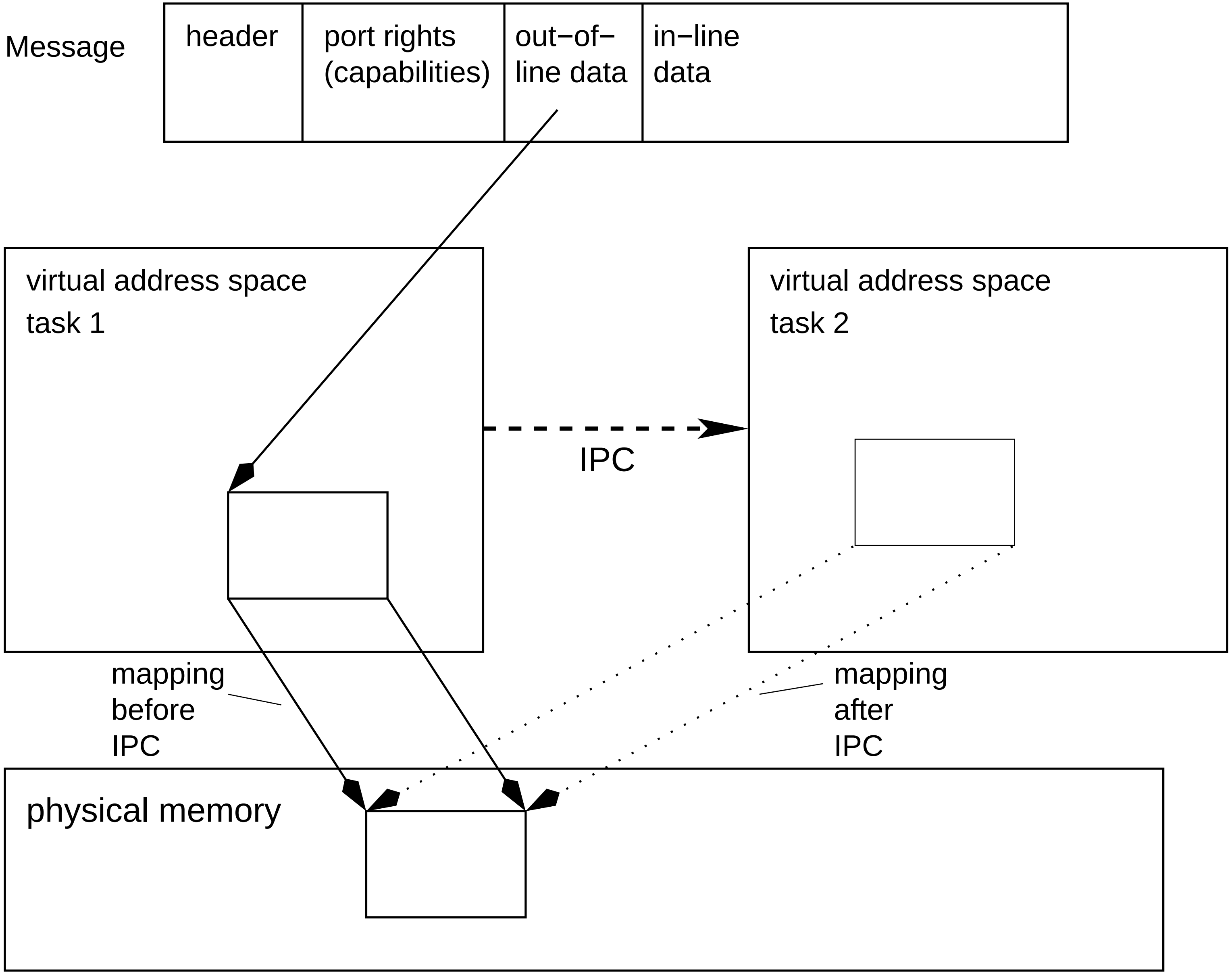
  - ⋆ possibly other capabilities
  - ⋆ “in-line” (by-value) data
  - ⋆ “out-of-line” (by reference) data, using copy-on-write,
    - ➜ may contain whole address spaces

MACH IPC


Message
header
port rights (capabilities)
out−of−line data
in−line data
virtual address space task 1
virtual address space task 2
IPC
mapping before IPC
mapping after IPC
physical memory

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    - ➜ inheriting from “blueprint” (as in Linux clone()),
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    - ➜ allocated automatically by kernel during IPC
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  - ⋆ 3 page states:
    - ➜ unallocated,
    - ➜ allocated & unreferenced,
    - ➜ allocated & initialised

COPY-ON-WRITE IN MACH

- When data is copied (“blueprint” or passed by-reference):
  - ➜ source and destination share single copy,
  - ➜ both virtual pages are mapped to the same frame
- Marked as read-only
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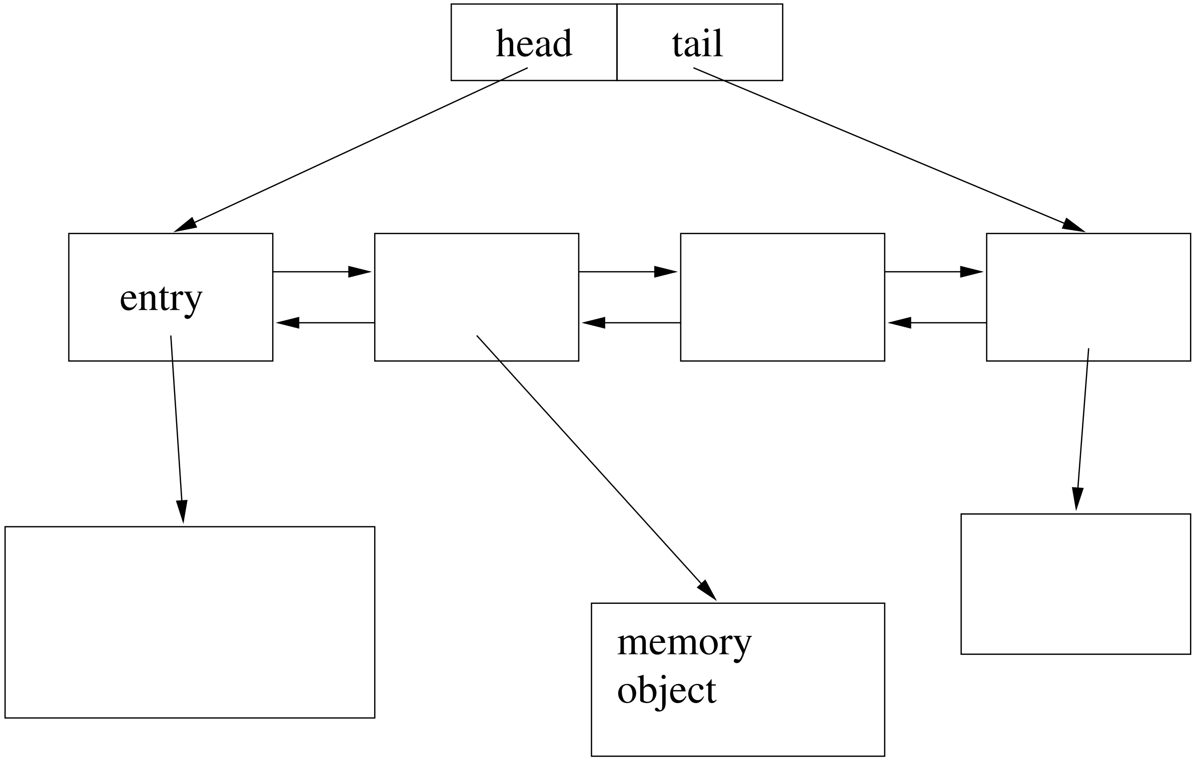
- Drawbacks:
  - ➜ expensive for small amounts of data (page table manipulations)
  - ➜ data must be properly aligned

MACH ADDRESS MAPS

- Address spaces represented as *address maps*:



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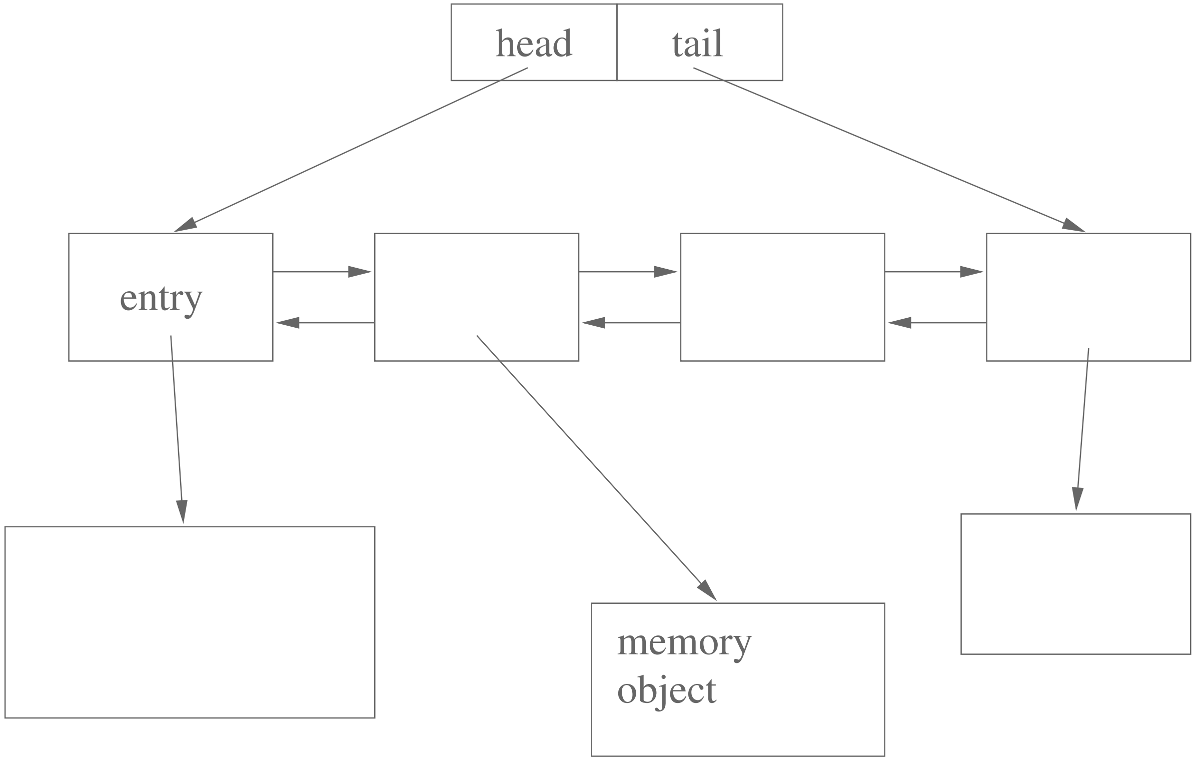


- Any part of AS can be mapped to (part of) a memory object
- Compact representation of *sparse* address spaces

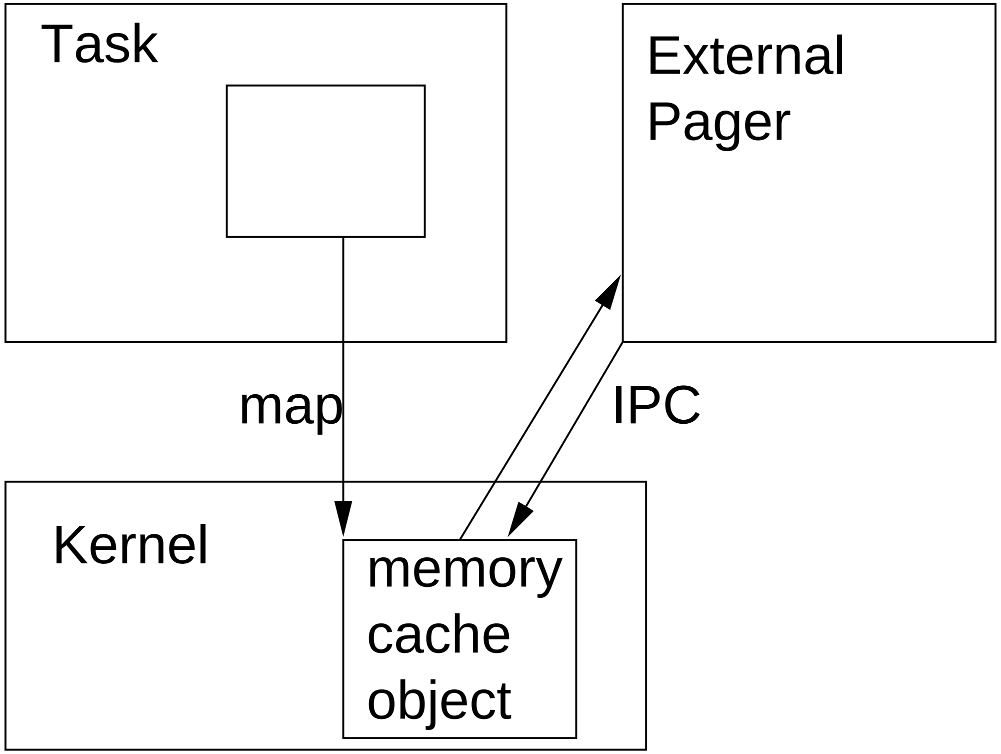
➜ Compare to multi-level page tables?

MEMORY OBJECTS

- Kernel doesn’t support file system
- Memory objects are an abstraction of secondary storage:
  - ⋆ can be mapped into virtual memory
  - ⋆ are cached by the kernel in physical memory
  - ⋆ pager invoked if uncached page is touched
    - ➜ used by file system server to provide data
- Support data sharing
  - ➜ by mapping objects into several address spaces
- Memory is only cache for memory objects

USER-LEVEL PAGE FAULT HANDLERS

- All actual I/O performed by *pager*; can be
  - ➜ default pager (provided by kernel), or
  - ➜ *external* pager, running at user-level.



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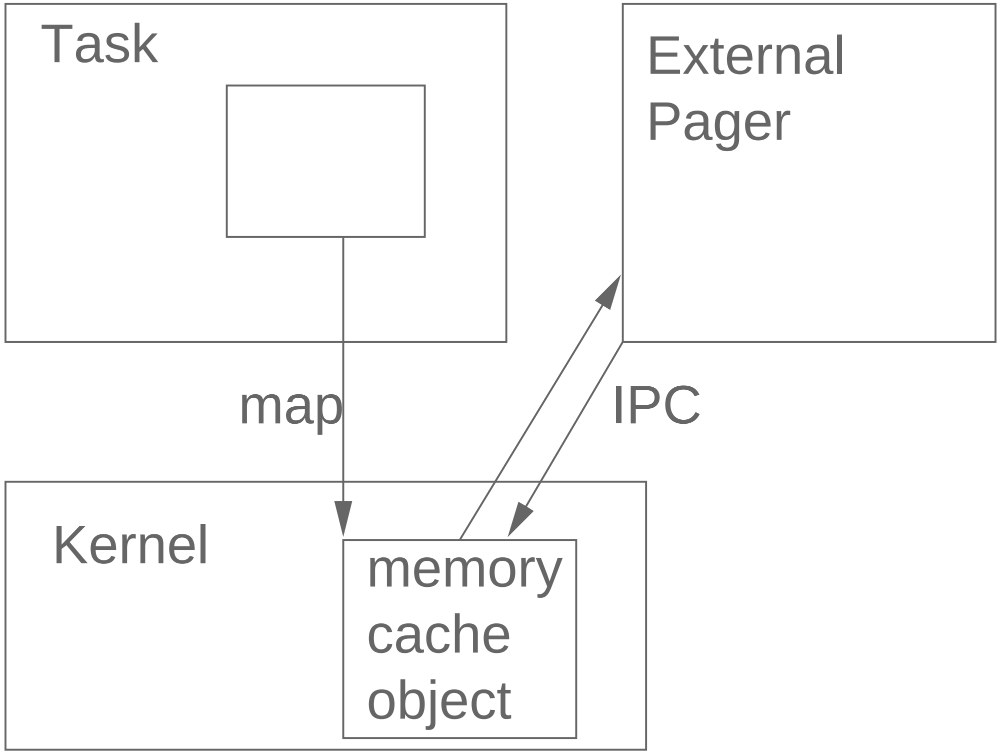


- Intrinsic page fault cost: 2 IPCs

HANDLING PAGE FAULTS

① Check protection & locate memory object
  ➜ uses address map

② Check cache, invoke pager if cache miss
  ➜ uses a hashed page table

③ Check copy-on-write
  ➜ perform physical copy if write fault

④ Enter new mapping into H/W page tables

REMOTE COMMUNICATION

- Client A sends message to server B on remote node

  ① A sends message to local *proxy port* for B's receive port

  ② User-level *network message server* receives from proxy port

  ③ NMS converts proxy port into (global) *network port*.

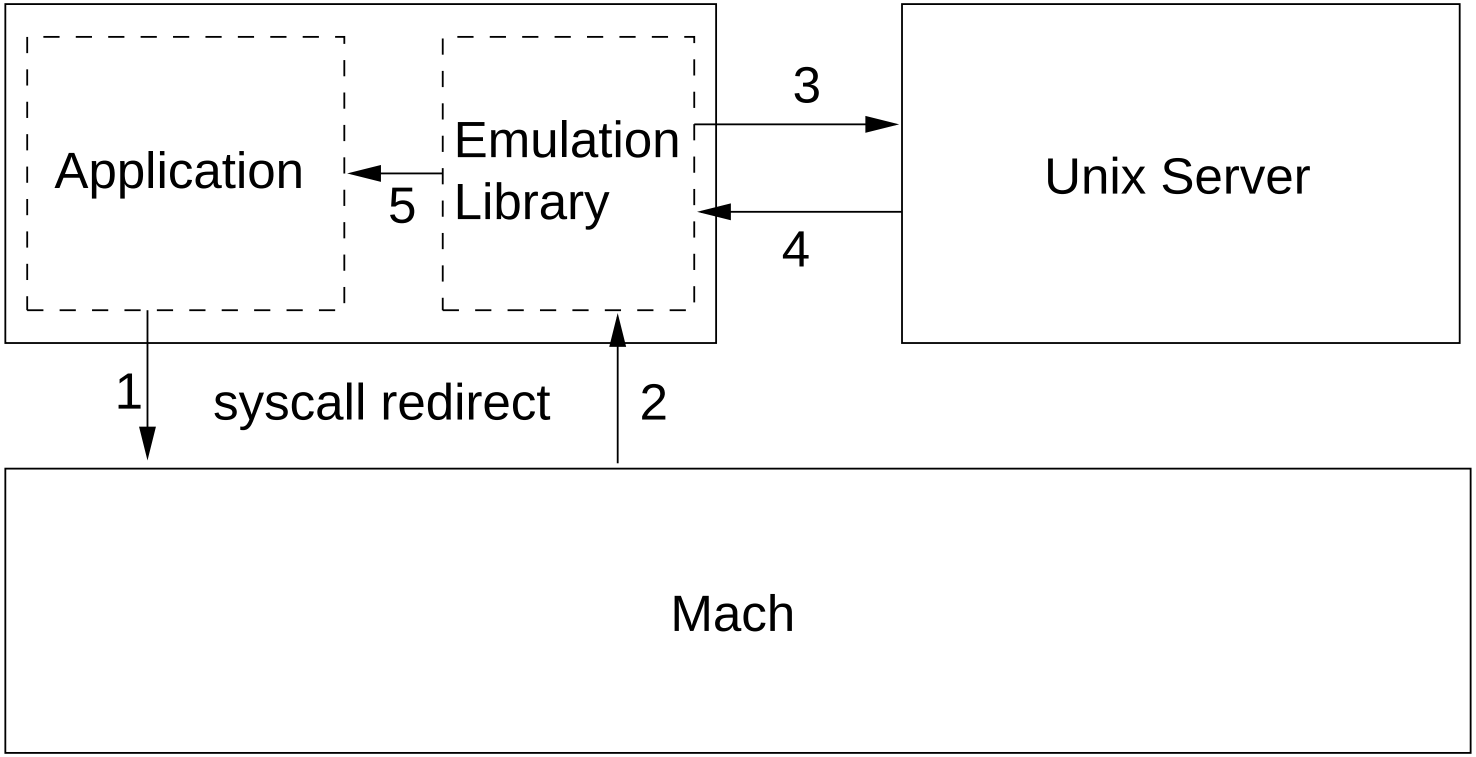
  ④ NMS sends message to NMS on B's node

  ➜ may need conversion (byte order...)

  ⑤ Remote NMS converts network port into local port (B's).

  ⑥ Remote NMS sends message to that port

MACH UNIX EMULATION



- Emulation library in user address space handles IPC
- Invoked by system call redirection (*trampoline mechanism*)
  ➜ supports binary compatibility

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Further information on Mach: [YTR$^+$87, CDK94, Sin97]

OTHER CLIENT-SERVER SYSTEMS

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- Most notable systems:

Amoeba: FU Amsterdam, early 1980's [TM81, TM84, MT86]

Chorus: INRIA (France), from early 1980's [DA92, RAA$^+$90, RAA$^+$92]

➜ Commercialised by *Chorus Systèmes* in 1988
➜ Recently bought by Sun

Windows NT: Microsoft (early 1990's) [Cus93]

➜ Main servers run in kernel mode

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Is Linus right?

MICROKERNEL PERFORMANCE

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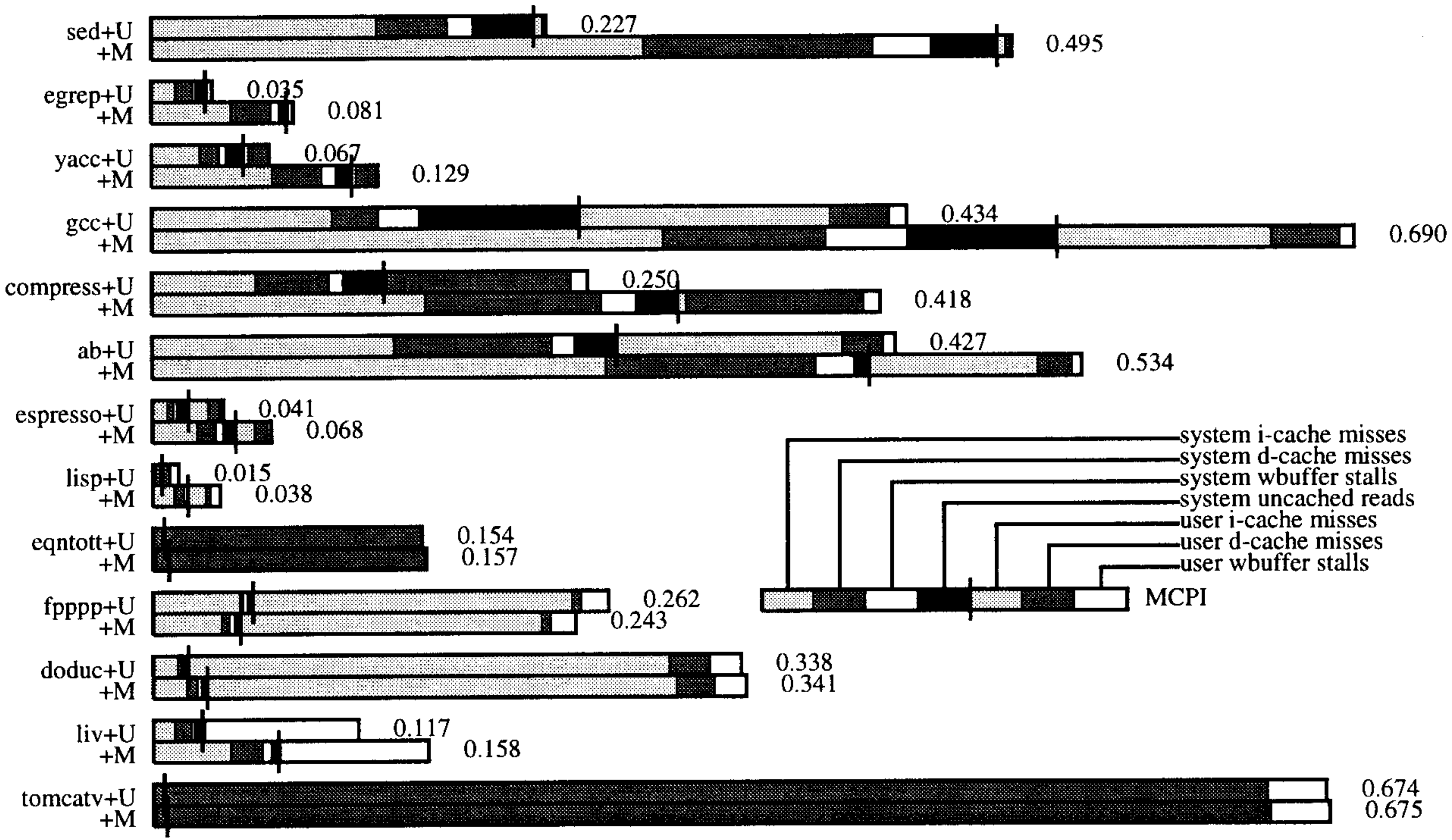
- First generation μ-kernel systems exhibited poor performance when compared to monolithic UNIX implementations
  - ➜ particularly Mach, the best-known example
- Reasons are investigated by [Chen & Bershad 93]:
  - ➜ instrumented user and system code to collect execution traces
  - ➜ run on DECstation 5000/200 (25MHz R3000)
  - ➜ run under Ultrix and Mach with Unix server
  - ➜ traces fed to memory system simulator
  - ➜ analyse MCPI (memory cycles per instruction)
    - ➜ baseline MCPI (i.e. excluding idle loops)

ULTRIX VS. MACH MCPI



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Claim:

- Degraded performance is (intrinsic?) result of OS structure
- IPC cost (known to be high in Mach) is not a major factor [Ber92]

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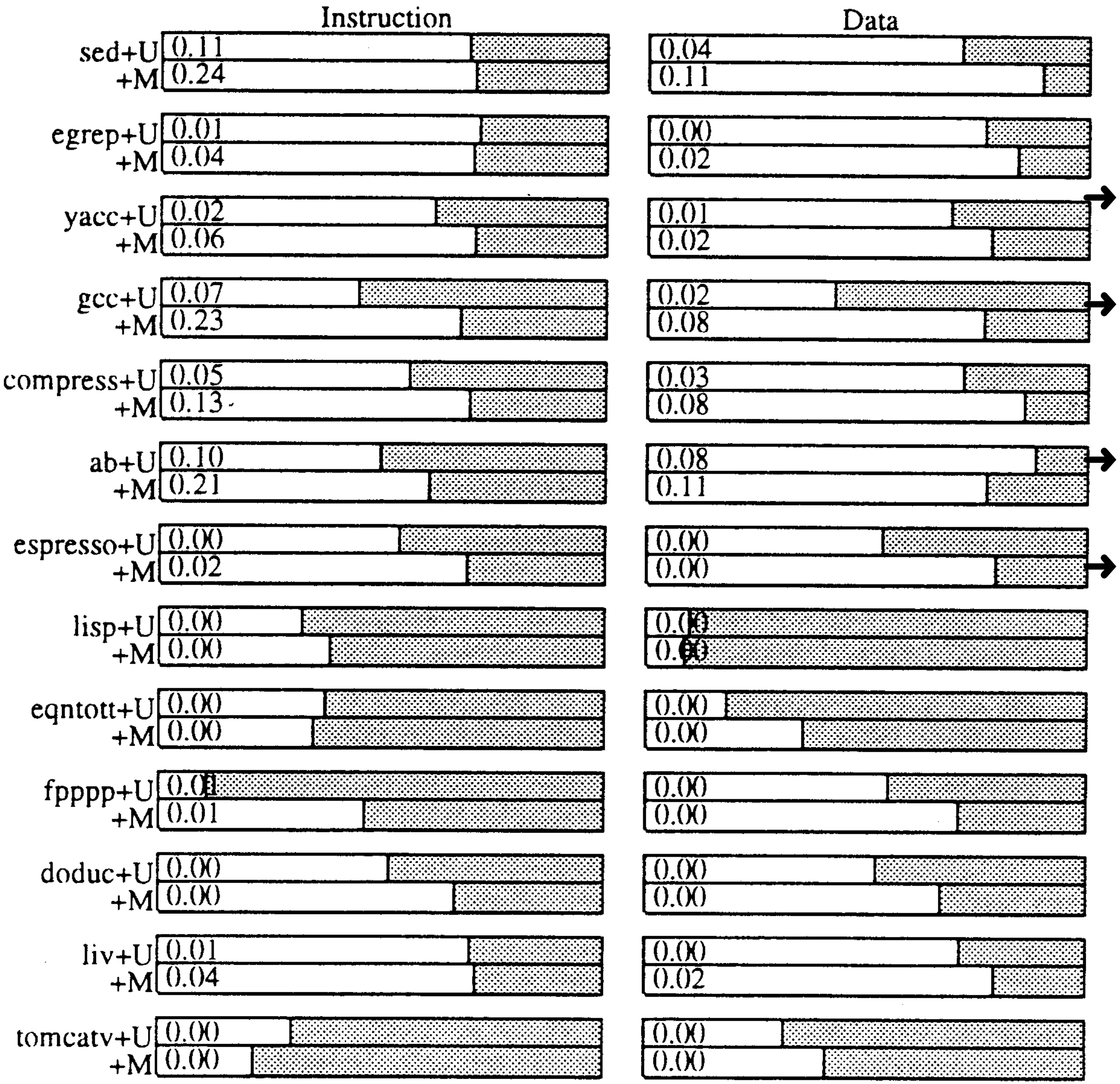
3 Competition between user and system code is not a problem

- ➜ Few conflicts between user and system caching
- ➜ TLB misses are not a relevant factor

Note: the hardware used has direct-mapped physical caches.
⇒ Split system/user caches wouldn't help

SELF INTERFERENCE



- Only examine system cache misses
- Shaded: System cache misses removed by associativity
- MCPI for system-only, using R3000 direct-mapped cache
- Reductions due to associativity were obtained by running system on a simulator and using a two-way associative cache of the same size

ASSERTIONS...

4 Self-interference is a problem in system instruction reference streams.

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7 **Virtual-to-physical mapping strategy can have significant impact on cache performance**

- ➜ Unfortunate mapping may increase conflict misses
- ➜ “Random” mappings (Mach) are to be avoided

OTHER EXPERIENCE WITH μ-KERNEL PERFORMANCE

- System call costs are (inherently?) high
  - ➜ Typically hundreds of cycles, 900 for Mach/i486
- Context (address-space) switching costs are (inherently?) high
  - ➜ Getting worse (in terms of cycles) with increasing CPU/memory speed ratios [Ous90]
  - ➜ IPC (involving system calls and context switches) is inherently expensive

SO, WHAT'S WRONG?

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SO, WHAT'S WRONG?

- μ-kernels heavily depend on IPC
- IPC is expensive
  - ⋆ Is the μ-kernel idea flawed?
  - ⋆ Should some code never leave the kernel?
  - ⋆ Do we have to buy flexibility with performance?

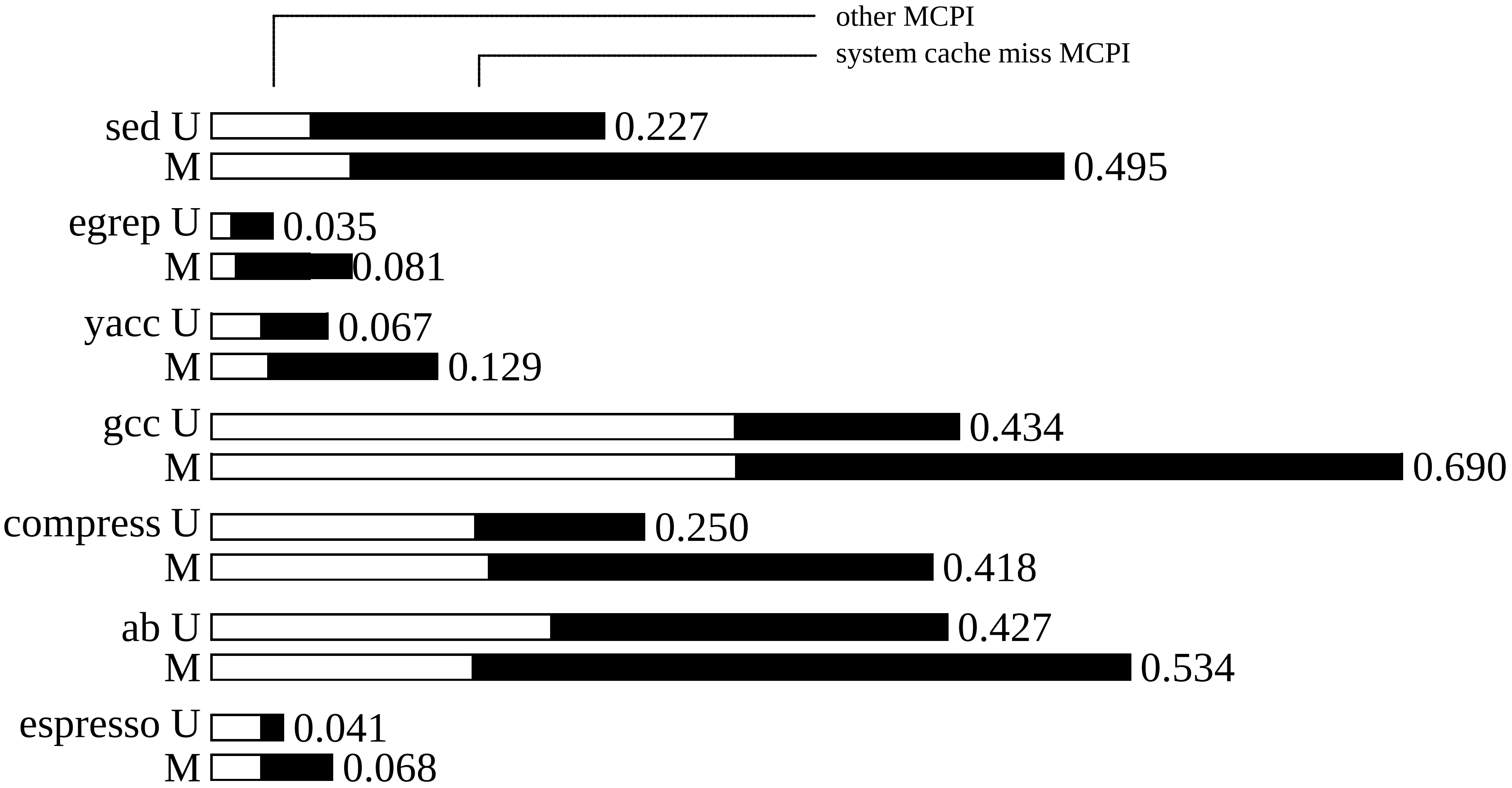
A CRITIQUE OF THE CRITIQUE

Data presented earlier:

- ➜ are specific to one (or a few) system,
- ➜ results cannot be generalised without thorough analysis,
- ➜ no such analysis has been done

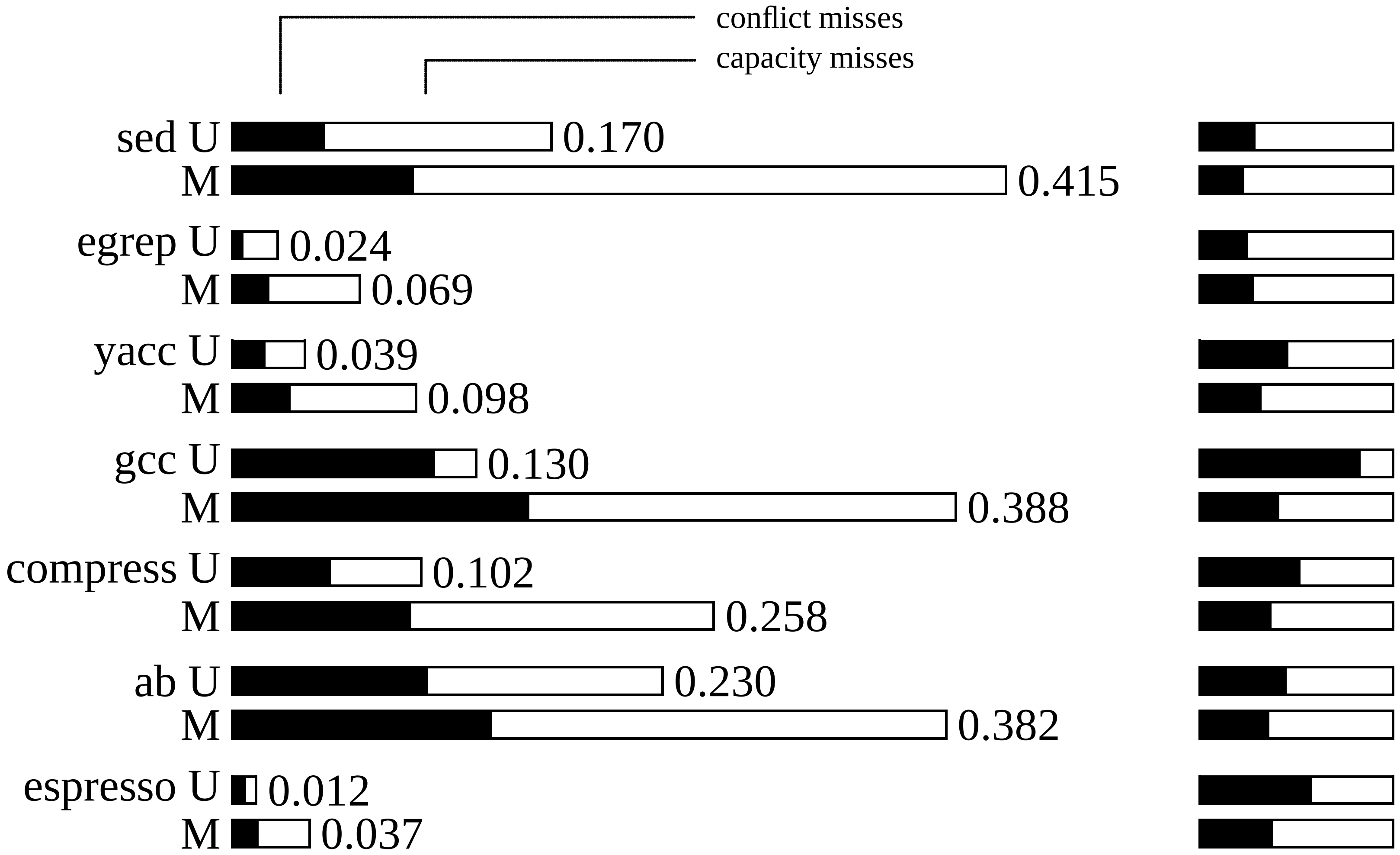
⇒ Cannot trust the conclusions [Lie95]

RE-ANALYSIS OF CHEN & BERSHAD'S DATA



MCPI for Ultrix and Mach

RE-ANALYSIS OF CHEN & BERSHAD'S DATA...



MCPI caused by cache misses: conflict (black) vs capacity (white)

CONCLUSION

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⇒ Mach μ-kernel working set is too big

Can we build μ-kernels which avoid these problems?

REQUIREMENTS FOR μ-KERNELS:

- Fast (system call costs, IPC costs)
- Small (big $\Rightarrow$ slow)

$\Rightarrow$ Must be well designed, providing a minimal set of operations.

Can this be done?

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⇒ Mach's performance is a result of design and implementation **not** the μ-kernel concept!

μ-KERNEL DESIGN PRINCIPLES [LIE96]

Minimality: If it doesn't *have to be* in the kernel, it *shouldn't* be in the kernel

Appropriate abstractions which can be made fast
and allow efficient implementation of services

Well written: It pays to shave a few cycles off
TLB refill handler or the IPC path

Unportable: must be targeted to specific hardware

- ➜ no problem if it's small, and higher layers are portable
- ➜ Example: Liedtke reports significant rewrite of memory management when porting from 486 to Pentium
- ⇒ "abstract hardware layer" is too costly

NON-PORTABILITY EXAMPLE: I486 VS PENTIUM:

- Size and associativity of TLB
- Size and organisation of cache (larger line size - restructured IPC)
- Segment regs in Pentium used to simulate tagged TLB

⇒ different trade-offs

WHAT *Must* A μ-KERNEL PROVIDE?

- Virtual memory/address spaces
- Threads
- *fast* IPC
- Unique identifiers (for IPC addressing)

μ-KERNEL DOES *Not* HAVE TO PROVIDE:

- File system
  - ➜ use user-level server (as in Mach)
- Device drivers
  - ➜ user-level driver invoked via interrupt (= IPC)
- Page-fault handler
  - ➜ use user-level pager

L4 IMPLEMENTATION TECHNIQUES (LIEDTKE)

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- General optimisations
  - ➜ “Hottest” kernel code is shortest
  - ➜ Kernel IPC code on single page, critical data on single page
  - ➜ Many H/W specific optimisations

MICROKERNEL PERFORMANCE

System	*CPU*	*MHz*	RPC μs	cyc/IPC	semantics
L4	R4600	100	1.7 μs	100	full
L4	Alpha	433	0.2 μs	45	full
L4	Pentium	166	1.5 μs	121	full
L4	486	50	10 μs	250	full
QNX	486	33	76 μs	1254	full
Mach	R2000	16.7	190 μs	1584	full
SCR RPC	CVAX	12.5	464 μs	2900	full
Mach	486	50	230 μs	5750	full
Amoeba	68020	15	800 μs	6000	full
Spin	Alpha 21064	133	102 μs	6783	full
Mach	Alpha 21064	133	104 μs	6916	full
Exo-tlrpc	R2000	116.7	6 μs	53	restricted
Spring	SparcV8	40	11 μs	220	restricted
DP-Mach	486	66	16 μs	528	restricted
LRPC	CVAX	12.5	157 μs	981	restricted

L4KA::PISTACHIO IPC PERFORMANCE

	port/	**C++**		**optimised**	
Architecture	**optimisation**	**intra AS**	**inter AS**	**intra AS**	**inter AS**
Pentium-3	UKa	180	367	113	305
Pentium-4	UKa	385	983	196	416
Itanium 2	UKa/NICTA	508	508	36	36
cross CPU	UKa	7419	7410	N/A	N/A
MIPS64	NICTA/UNSW	276	276	109	109
cross CPU	NICTA/UNSW	3238	3238	690	690
PowerPC-64	NICTA/UNSW	330	518	200‡	200‡
Alpha 21264	NICTA/UNSW	440	642	≈70†	≈70†
ARM/XScale	NICTA/UNSW	340	340	120–140‡	120–140‡
UltraSPARC	NICTA/UNSW			100‡	100‡

† “Version 2” assembler kernel

‡ Guestimate!

CASE IN POINT: L^4LINUX [HÄRTIG *et al*. 97]

- Port of Linux kernel to L4 (like Mach Unix server)
  - ➜ single-threaded (for simplicity, **not** performance)
  - ➜ is pager of all Linux user processes
  - ➜ maps emulation library and signal-handling code into AS
  - ➜ server AS maps physical memory (& Linux runs within)
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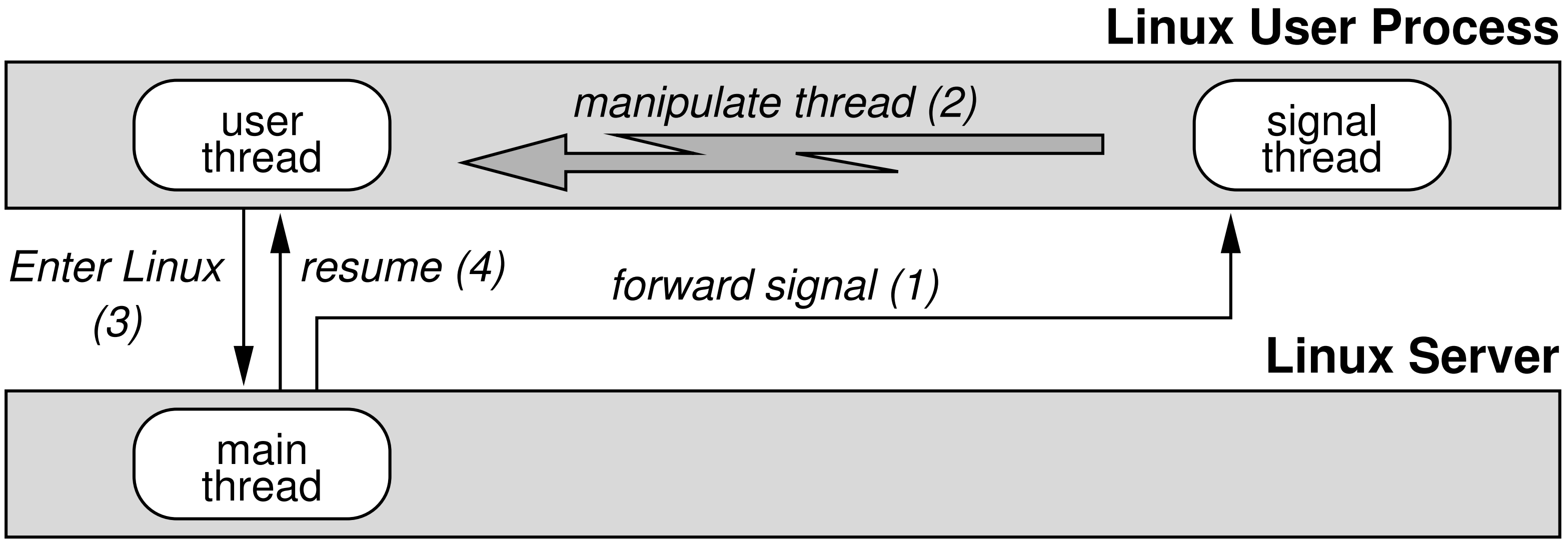
- Changes to Linux restricted to architecture-dependent part

- Duplication of page tables (L4 and Linux server)

- Binary compatible to native Linux via trampoline mechanism
  - ➜ but also modified `libc` with RPC stubs

SIGNAL DELIVERY IN L^{4}LINUX



- Separate signal-handler thread in each user process
  - ➜ server IPCs signal-handler thread
  - ➜ handler thread ex_regs main user thread to save state
  - ➜ user thread IPCs Linux server
  - ➜ server does signal processing
  - ➜ server IPCs user thread to resume

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System	*Time [μs]*	*Cycles*
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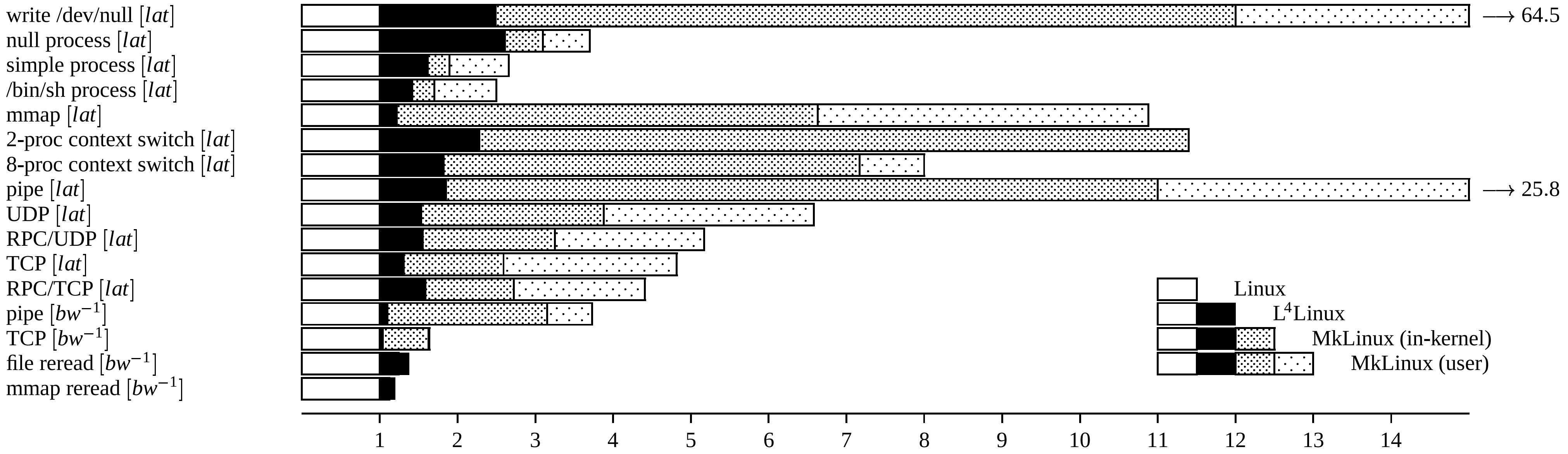
CYCLE BREAKDOWN:

Client	*Cycles*	*Server*
enter emulation lib	20	
send syscall message	168	wait for msg
	131	Linux kernel
receive reply	188	send reply
leave emulation lib	19	

Hardware cost: 82 cycles (133MHz Pentium)

L^{4}LINUX PERFORMANCE

MICROBENCHMARKS: LMBENCH



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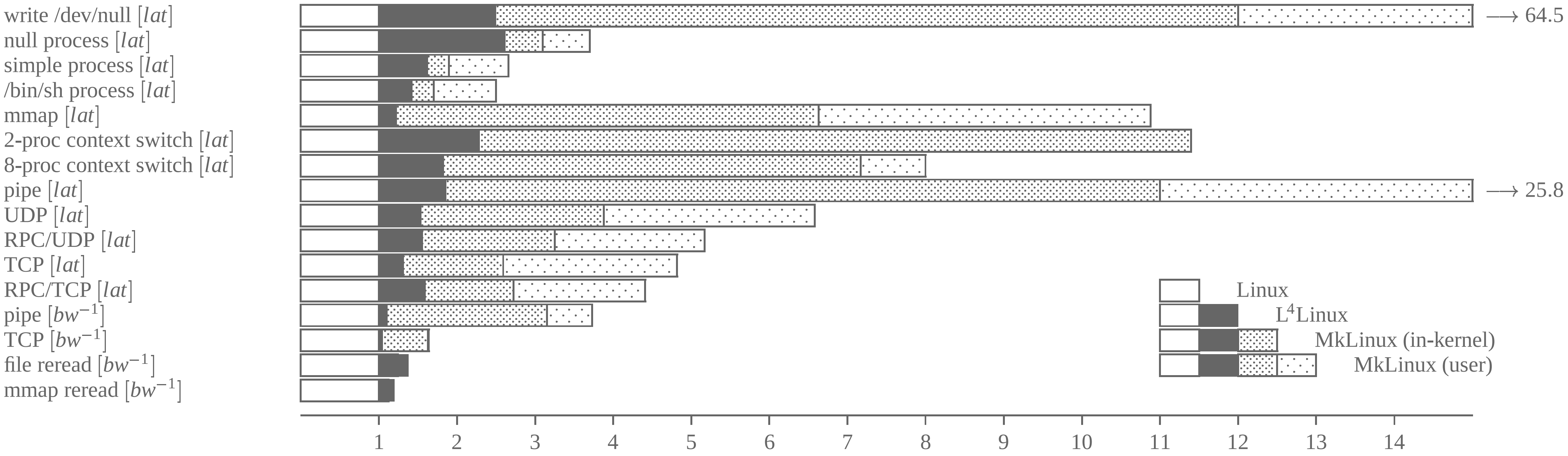
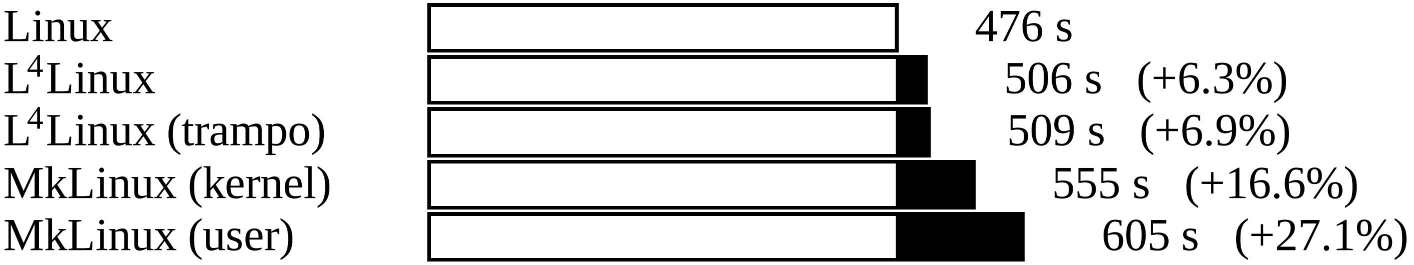


MACROBENCHMARKS: KERNEL COMPILE



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- Mach sux $\not\Rightarrow$ microkernels suck
- L4 shows that performance *might* be deliverable
  - ➜ L^4Linux gets close to monolithic kernel performance
  - ➜ need real multi-server system to evaluate μ-kernel potential
- Jury is still out!
- Mach has prejudiced community (see Linus...)
  - ➜ It's still an uphill battle!

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