Power Management
Selected Issues

COMP9242 2007/S2 Week 8

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Laptops

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  ➜ maximise battery lifetime

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- Approaches:
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    - ➜ trade-off with response time
  - ➜ put peripherals into low-power mode when idle
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  - ➜ reduce clock frequency

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    - why does this help?

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  - ➜ for air conditioning

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  - ➜ for computer power supply
  - ➜ for air conditioning
- Approaches:
  - ➜ reduce clock frequency
  - ➜ spin down disks
  - ➜ shut down nodes
    - use virtualization to migrate load

General Power Management Issues

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  - ➜ transitioning between power modes takes time
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  - ➜ if transitioning too aggressively may consume more energy
  - ➜ rule of thumb for transition to low-power mode:
    - transition when wasted energy exceeds transitioning cost

Low-power modes

- Disk:
  - ➜ spin down

Low-power modes

- Disk:
  - ➜ spin down
- Memory:
  - ➜ loss-free low-power state
    - content not accessible until return to normal state
    - fast transition
    - moderate savings
  - ➜ destructive low-power state
    - content lost
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- CPU:
  - ➜ dynamic voltage and frequency scaling (DVFS)

Dynamic Voltage and Frequency Scaling

Basis of DVFS:

1. DRAM circuits draw power only when switching
   - ➜ switching energy (approximately) constant per clock cycle:

$$P = VI \propto V^2$$

   - ➜ switches per second = core frequency:

$$P \propto f$$

   - ➜ overall:

$$P(f) \propto fV^2$$

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2. DRAM circuits switch faster under higher voltage
   - ➜ can reduce voltage at lower frequencies (to a limit):

$$V_{min} \text{ monotonic in } f$$

$$P_{min} \propto f^2 \cdots f^3$$

Dynamic Voltage and Frequency Scaling

Basis of DVFS:

3. Work performed per clock cycle is independent of frequency
   - ➜ computation takes fixed number of cycles N
   - ➜ total computation time is:

$$T = N/f$$

   - ➜ energy for computation is:

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   ... independent of f!

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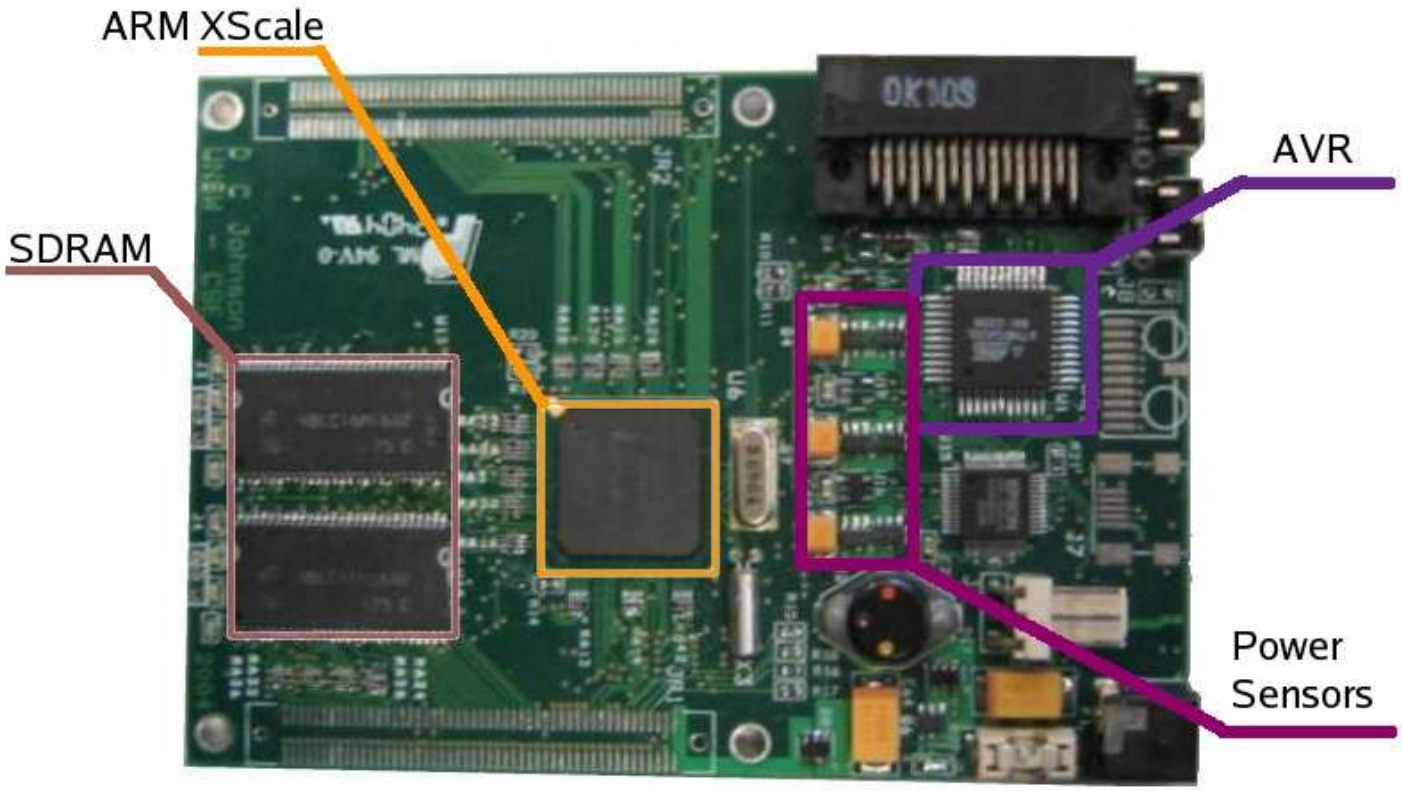
- **Let's have a look at real hardware!**

Hardware Platform

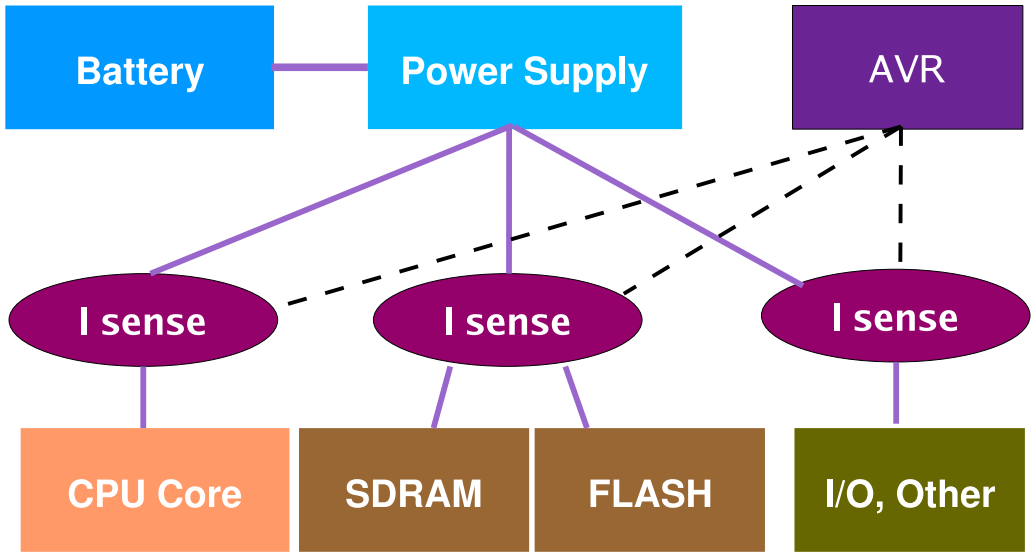
PLEB 2 (NICTA '05):

- Single board computer based on Intel XScale (PXA255)
- Representative of a typical embedded system



Hardware Platform

- Three power supplies: CPU, Memory and IO
- Each power supply's current is measured
- On-board micro-controller (AVR) for monitoring
- Samples taken periodically according to AVR clock
- $f_{\max}$ samples is 15 KHz, subdivided into three channels



PXA255 Voltage and Frequency Settings

Valid voltage/frequency configurations:

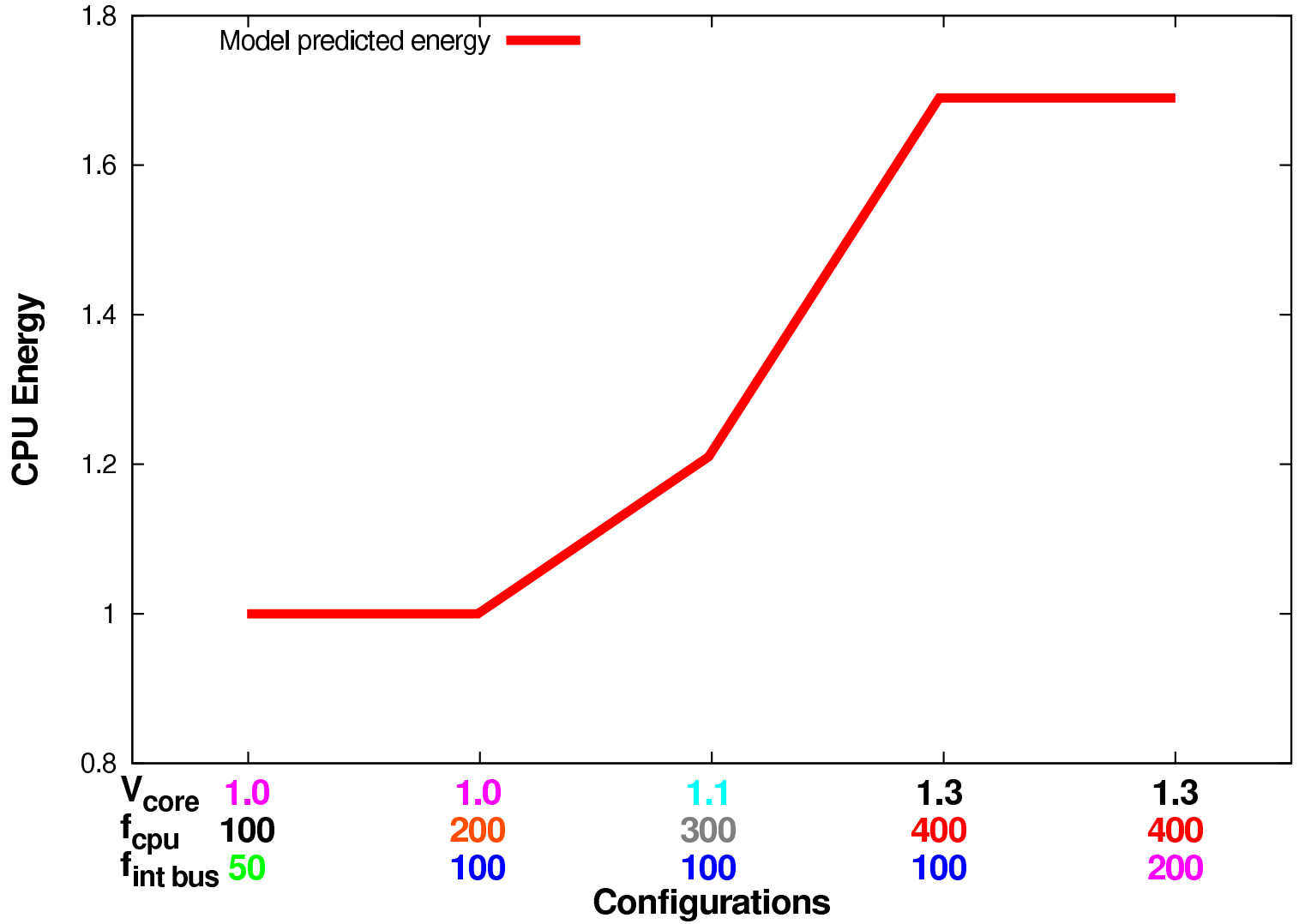
V_{core} (V)	f_{cpu} (MHz)	$f_{internalbus}$ (MHz)	f_{mem} (MHz)
1.0	100	50	100
1.0	200	100	100
1.1	300	100	100
1.3	400	100	100
1.3	400	200	100

Benchmarks

14 Macro benchmarks:

- ➜ most from MiBench, selected according to resource limitations
- ➜ automotive, industrial control, network, office, signal processing
- ➜ plus 4 more: gzip, MP3, image analysis, speech compression

1. Normalized CPU Energy Model



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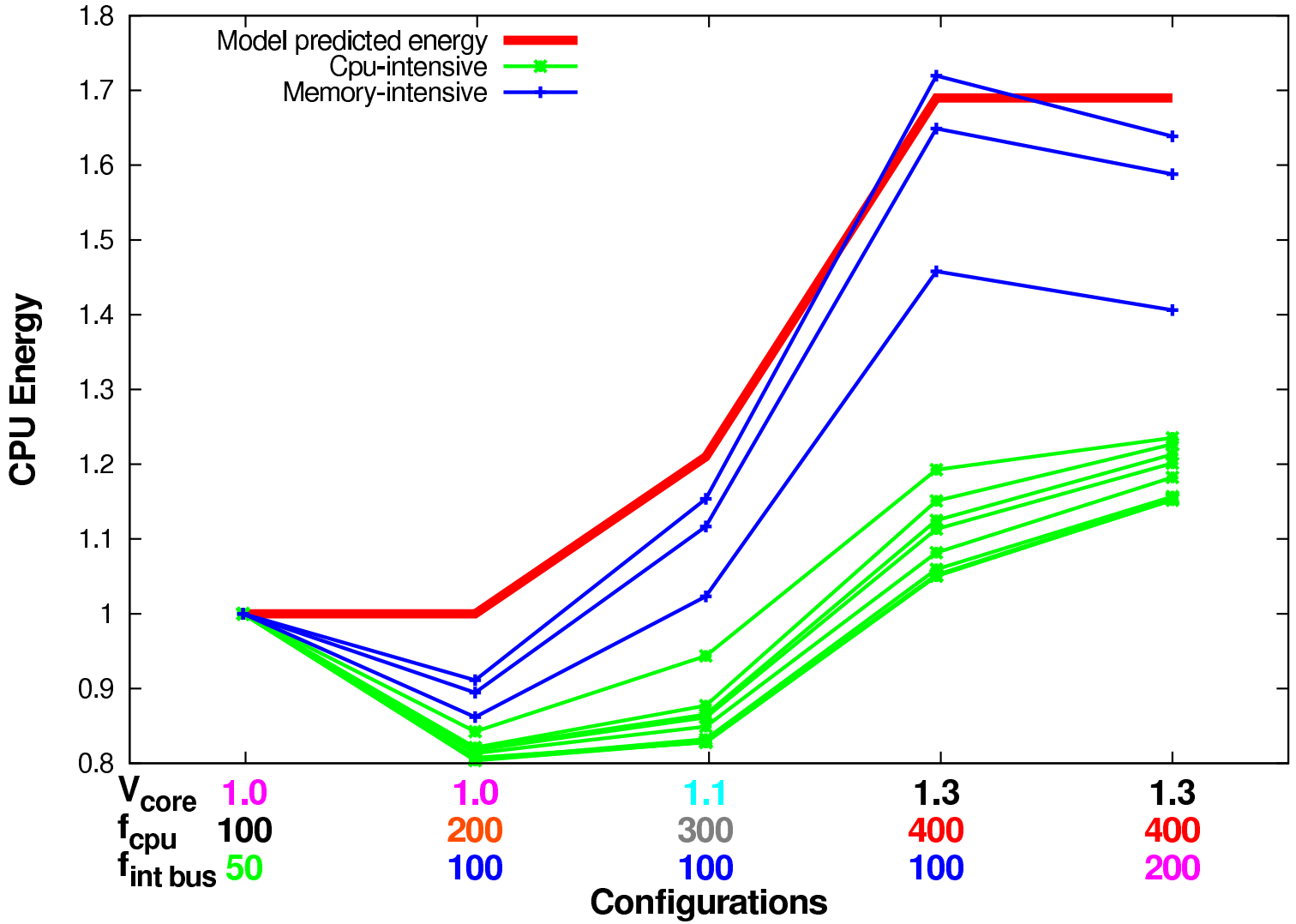
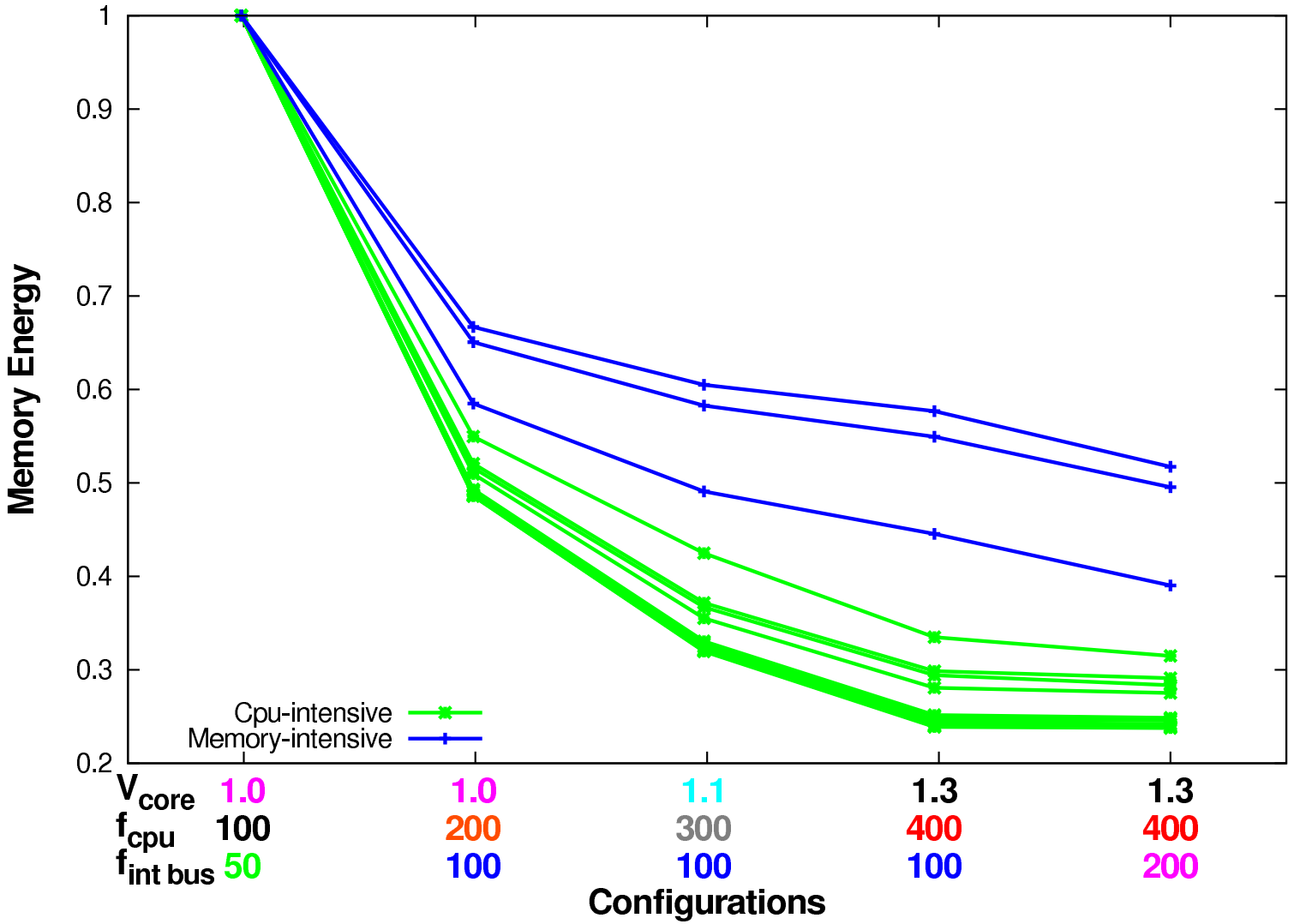
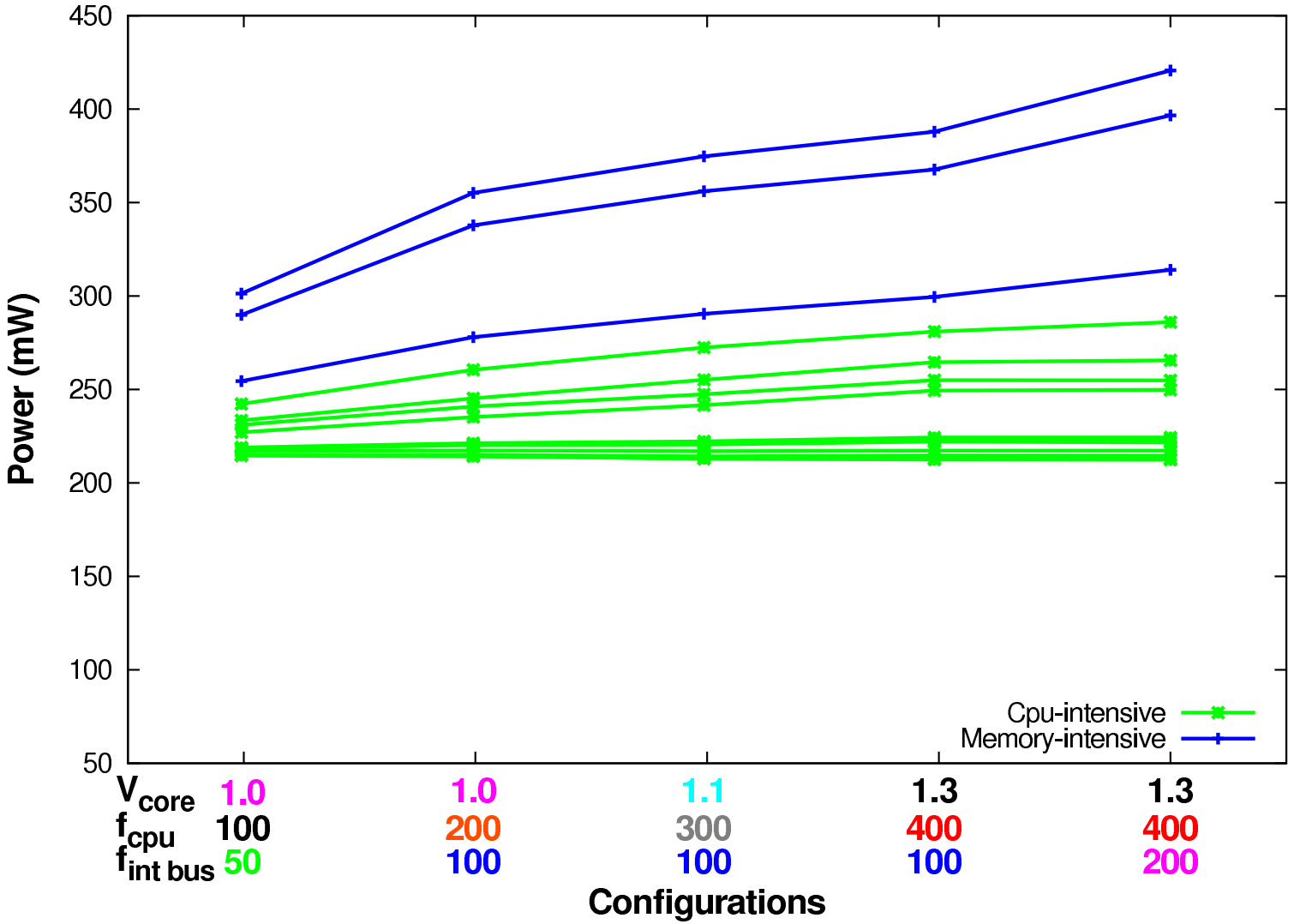


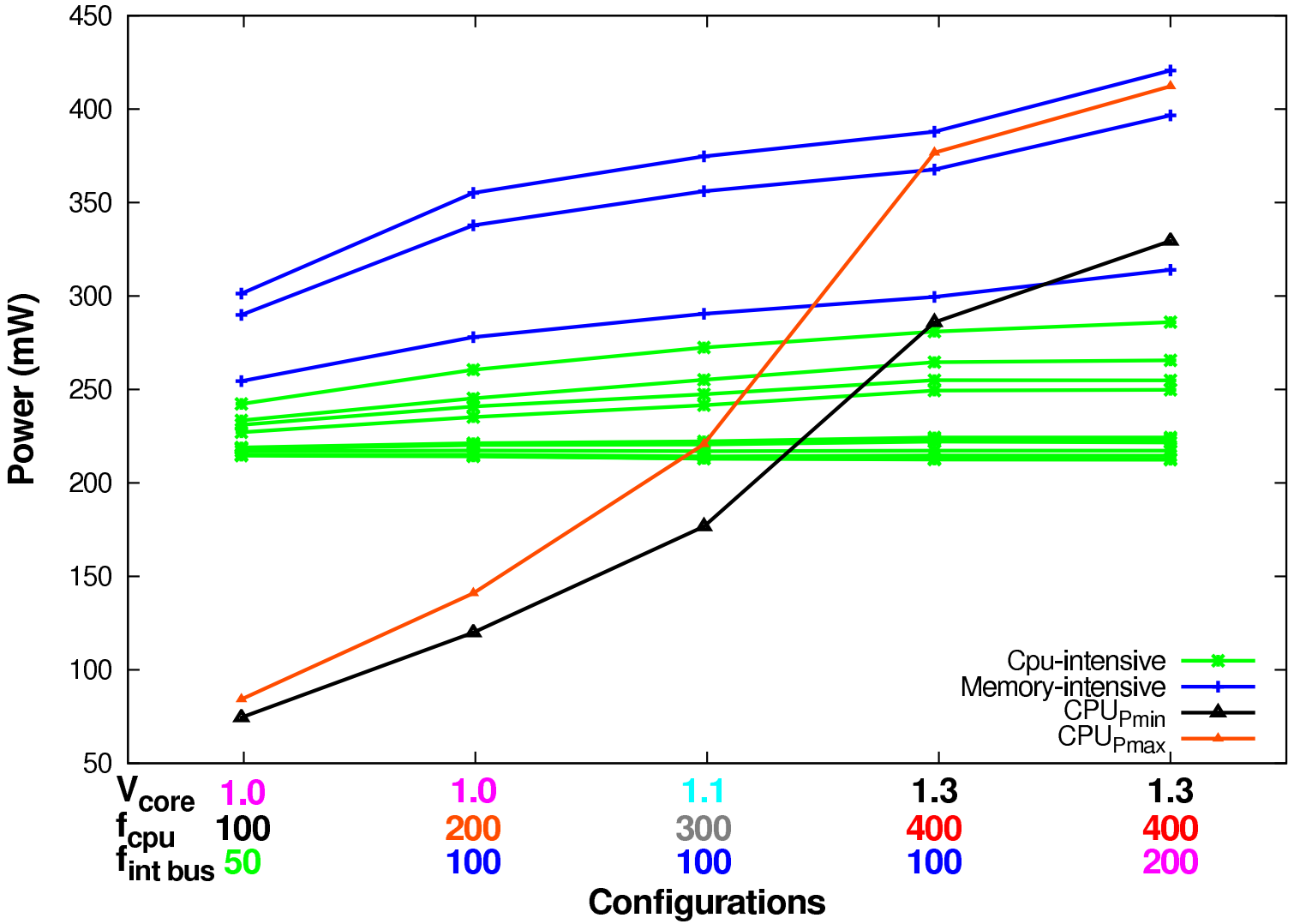
1.B Normalized Memory Energy



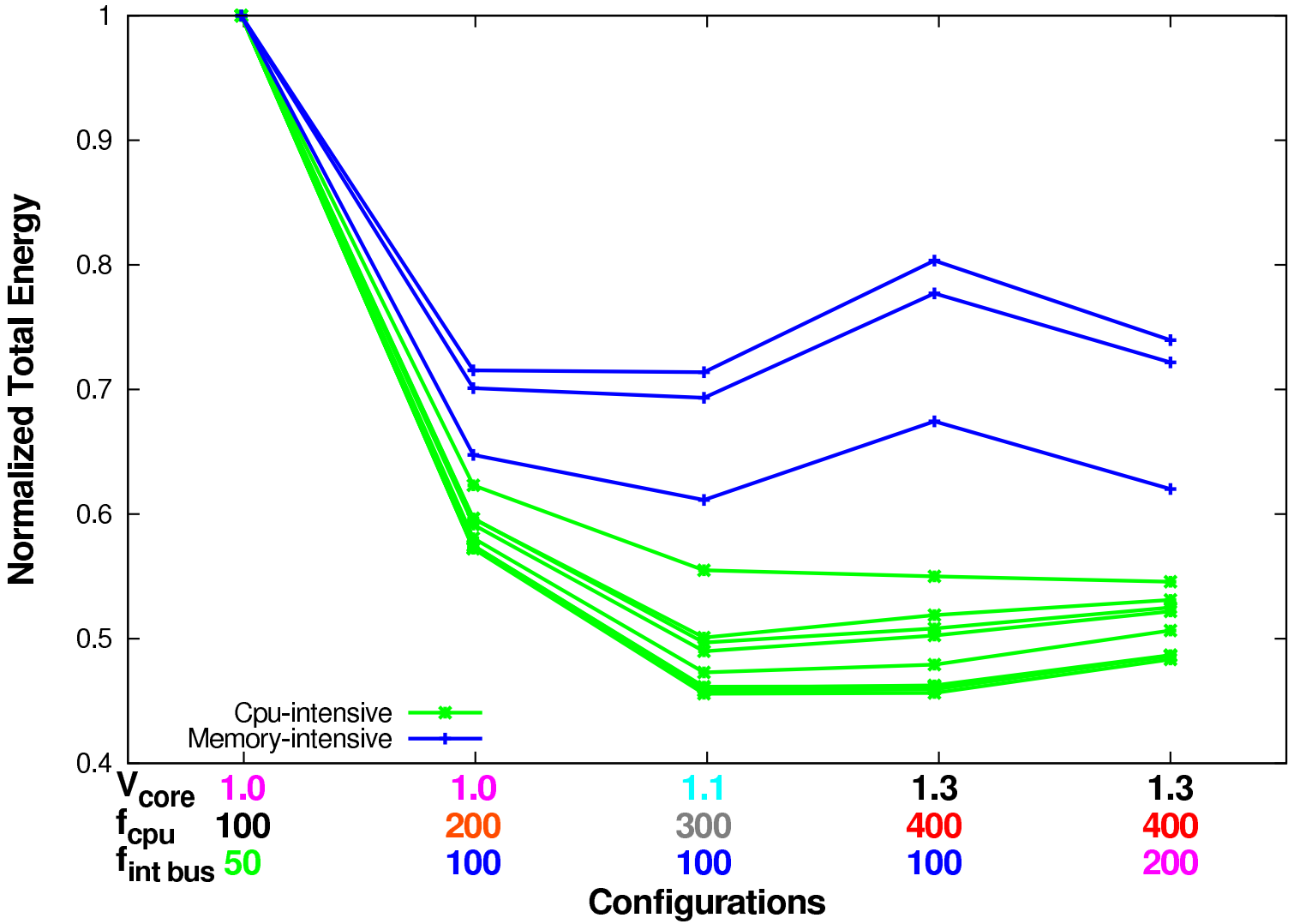
2. Memory Power



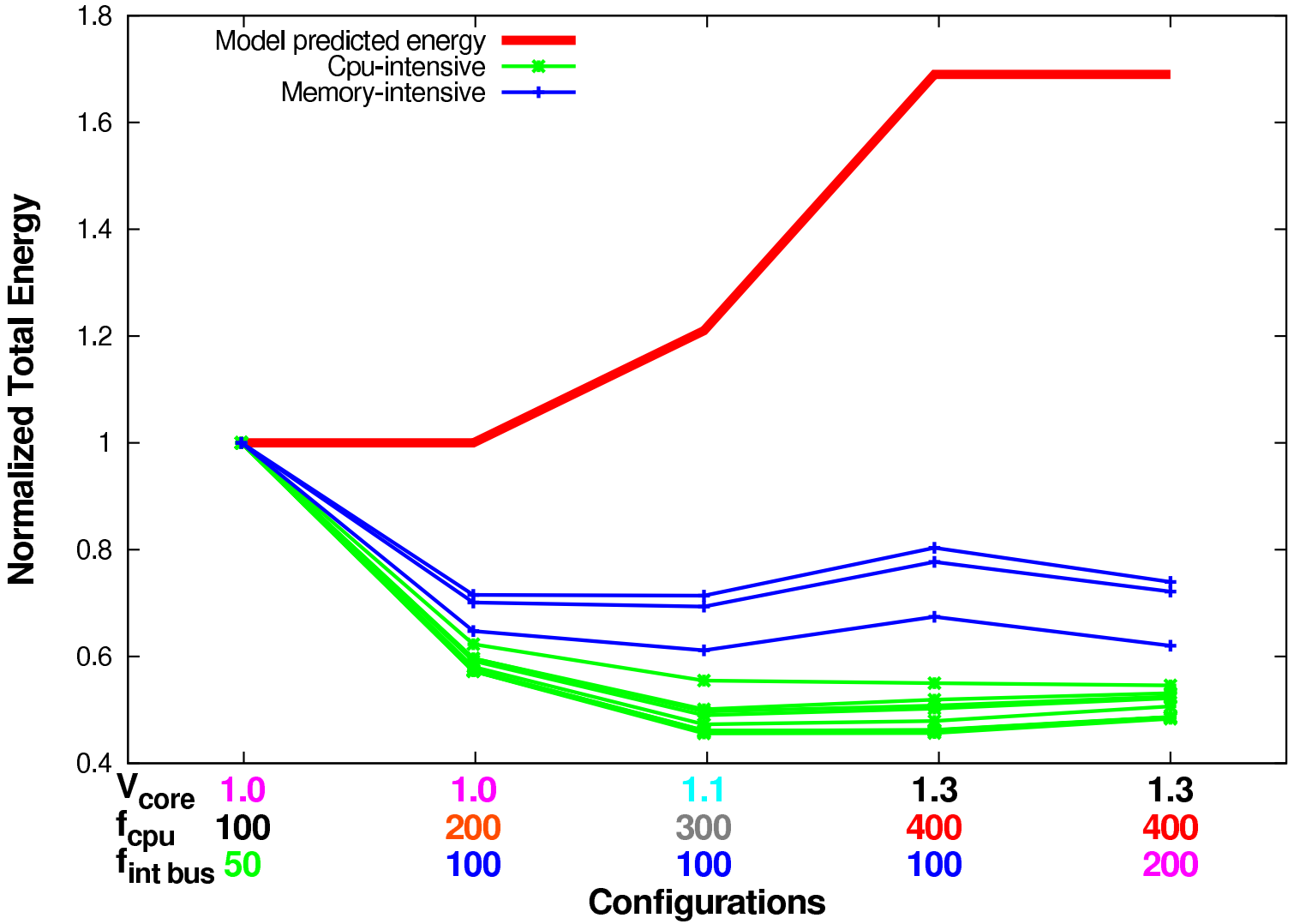
2. Memory Power vs CPU Power



3. Normalized Total Energy



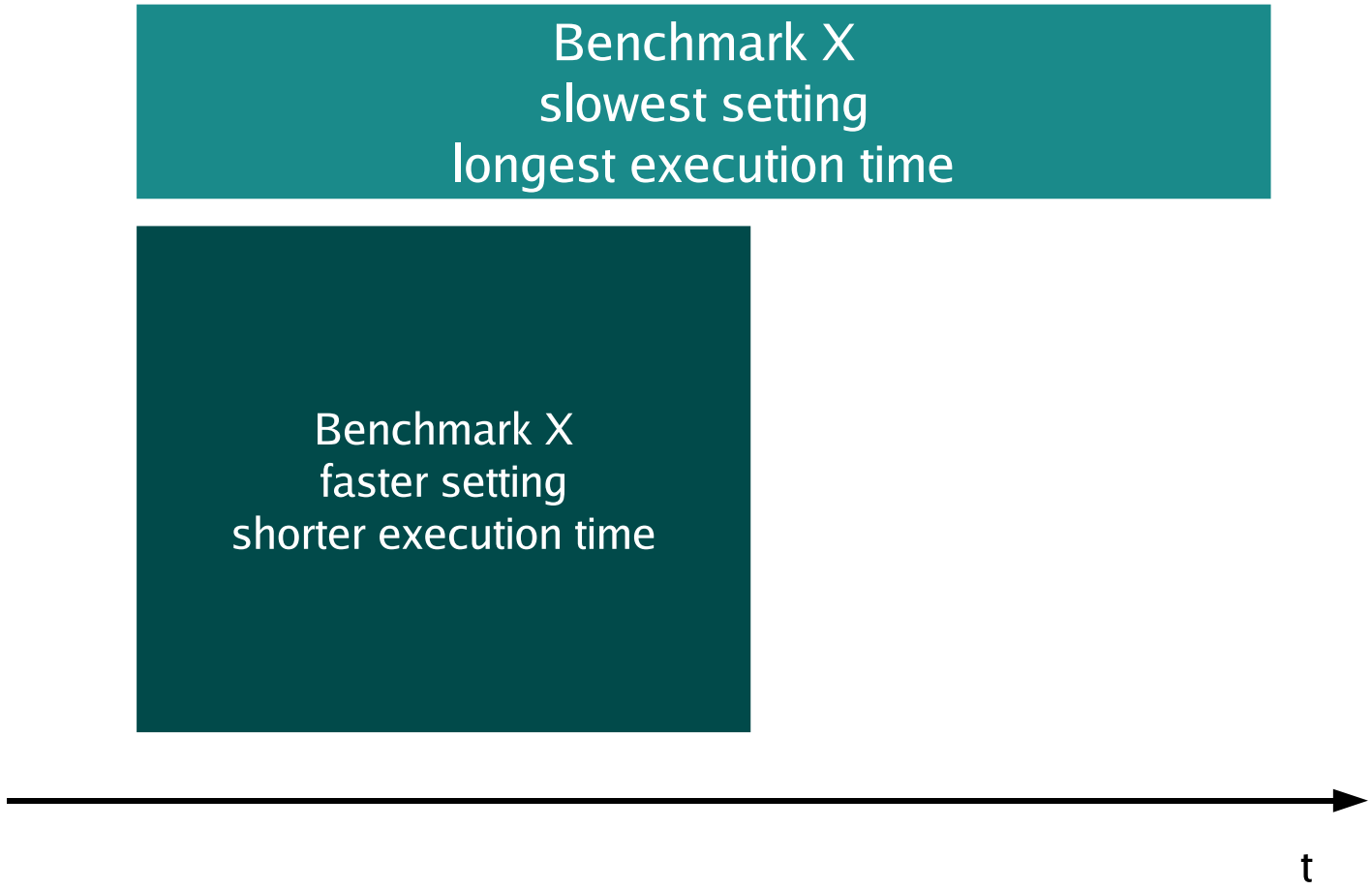
3. Normalized Total Energy vs Naive Model



Padding with idle power to equal total time

Benchmark X
slowest setting
longest execution time

Padding with idle power to equal total time



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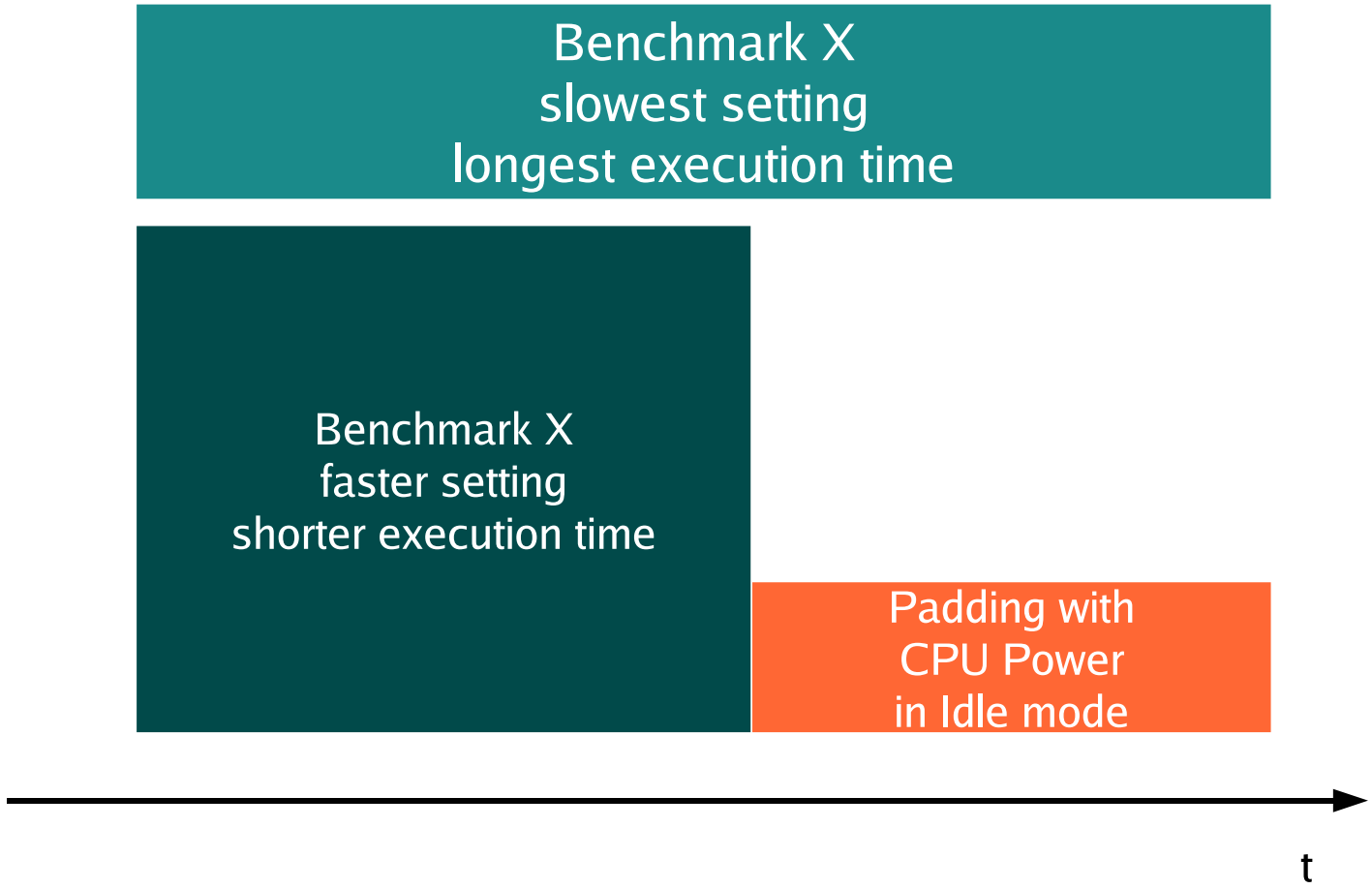
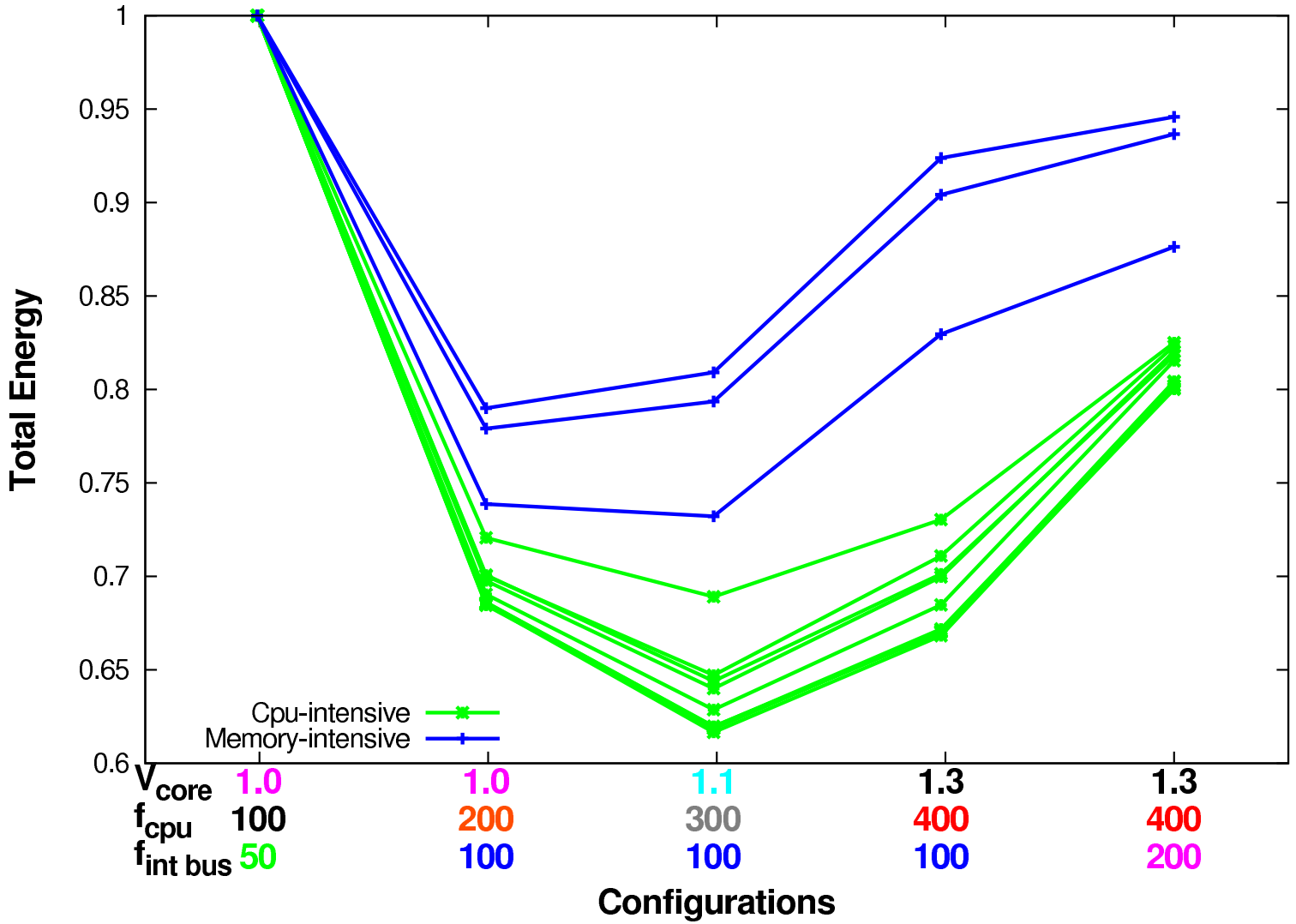


4. Normalised total energy padded to equal time



Memory Power Estimation

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- Model memory power via performance counters.
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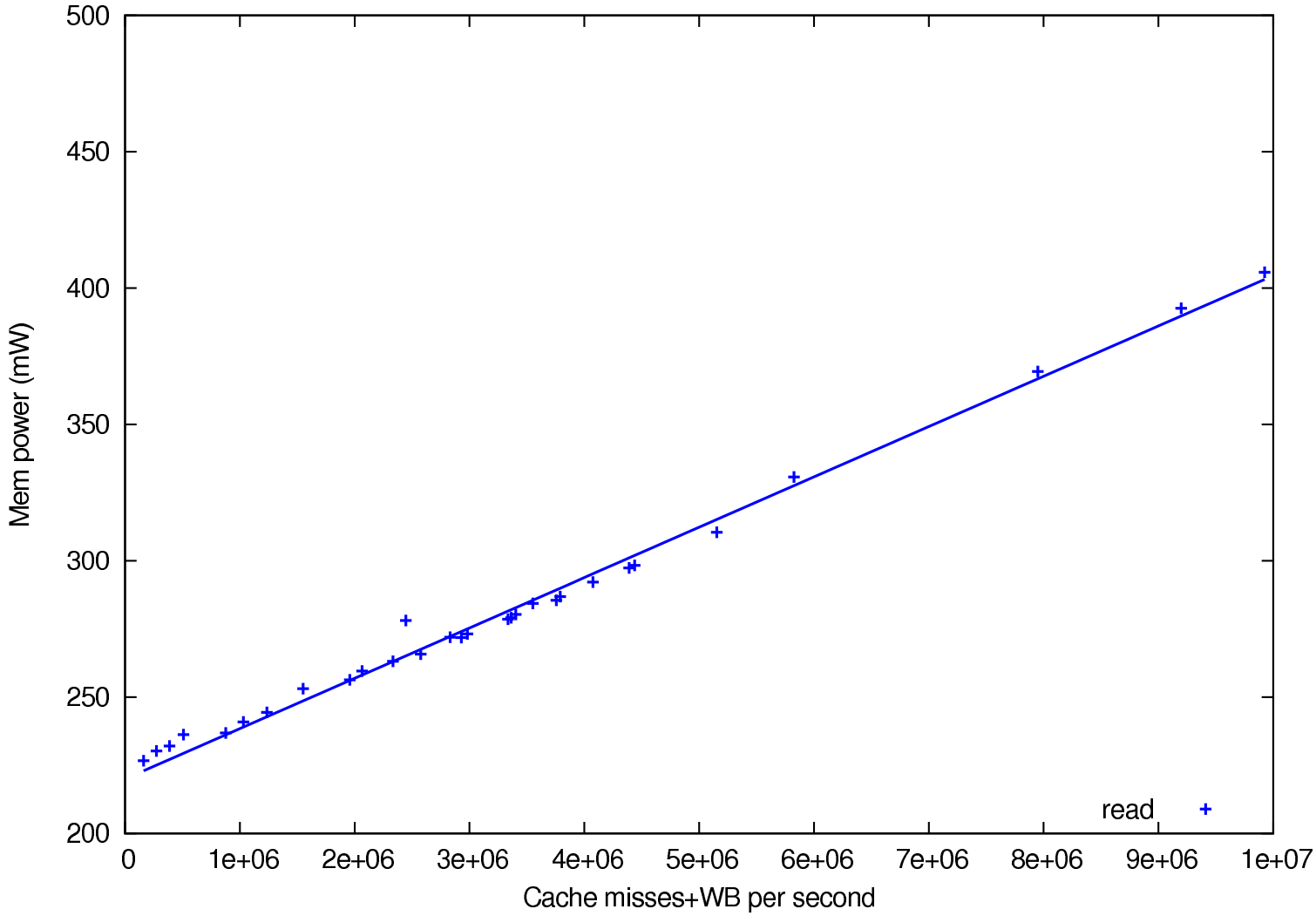
- Model memory power via performance counters.
- Counting memory accesses leads to good results (WB02)
- However, XScale doesn't have enough performance counters
- Idea: count cache misses instead?
- Investigated via two micro-benchmarks
  - *read*: only load instructions
  - *modify*: load and then store to same location

5. Memory power vs cache miss rate



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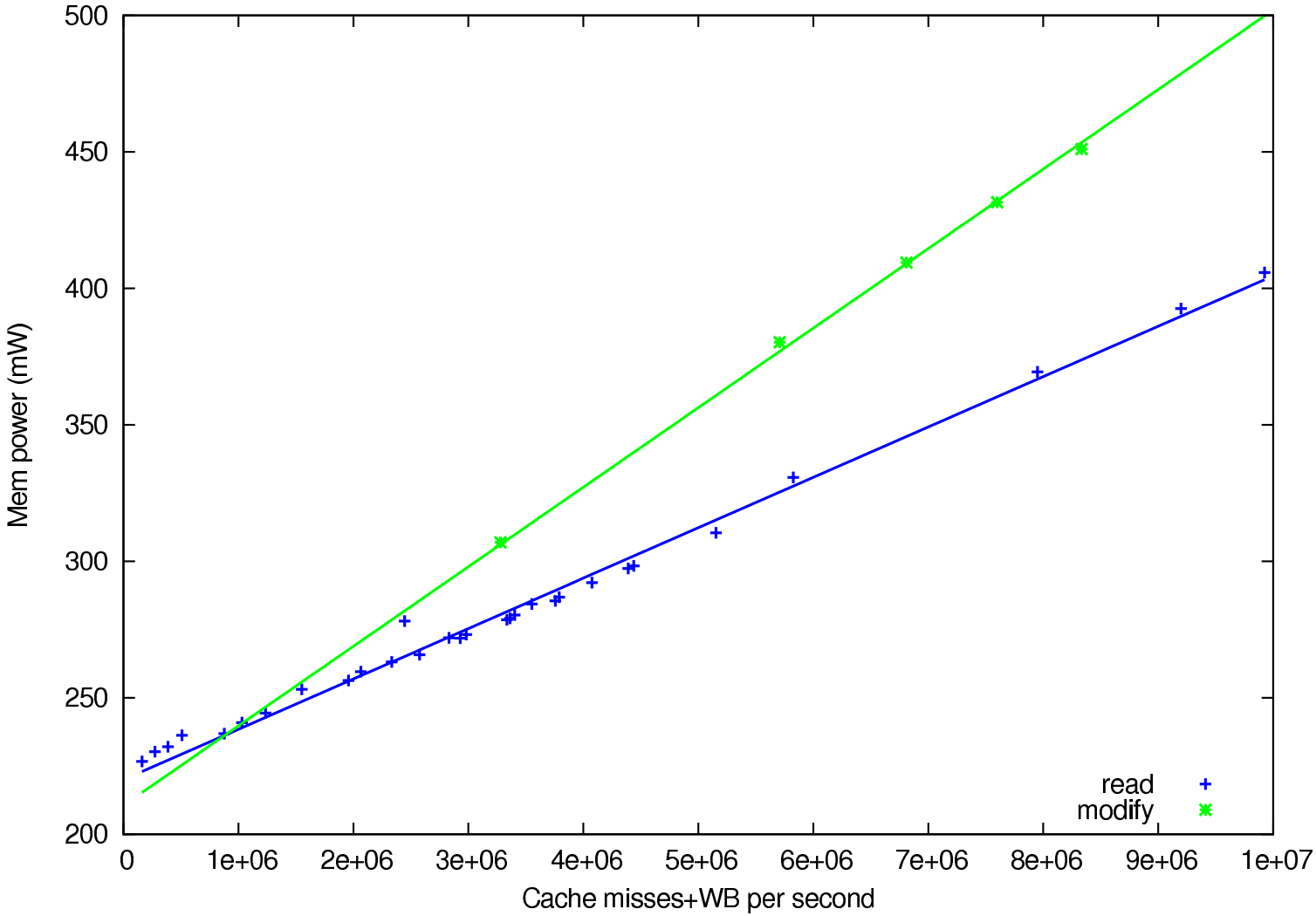

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  - ➜ memory stalls
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  - ➜ memory power (and I/O devices)
  - ➜ multiple frequency/voltage domains
- Things aren't as simple as some people think...
  - ➜ yet this model is used in many publications!

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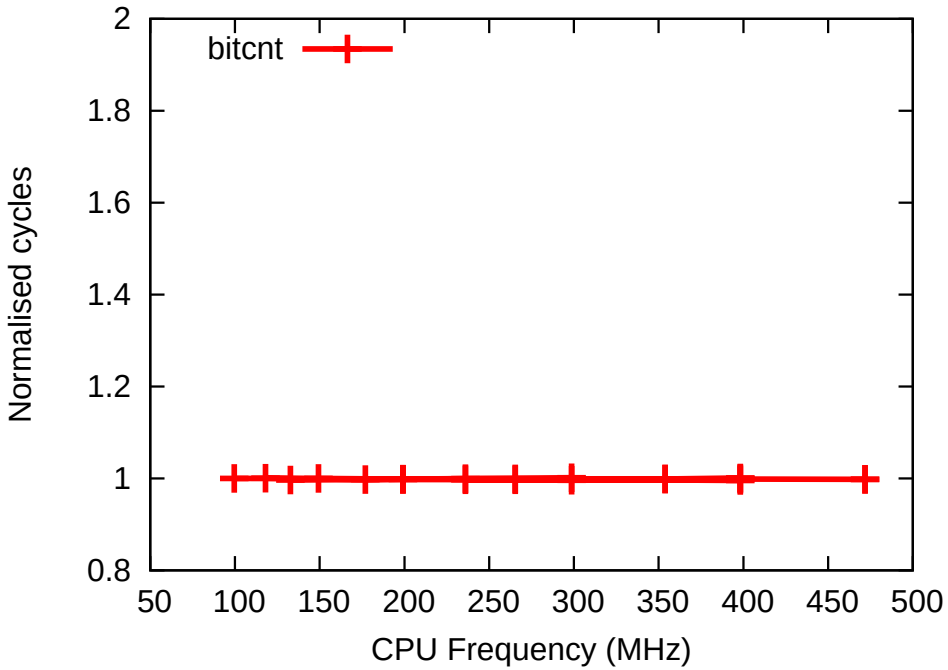

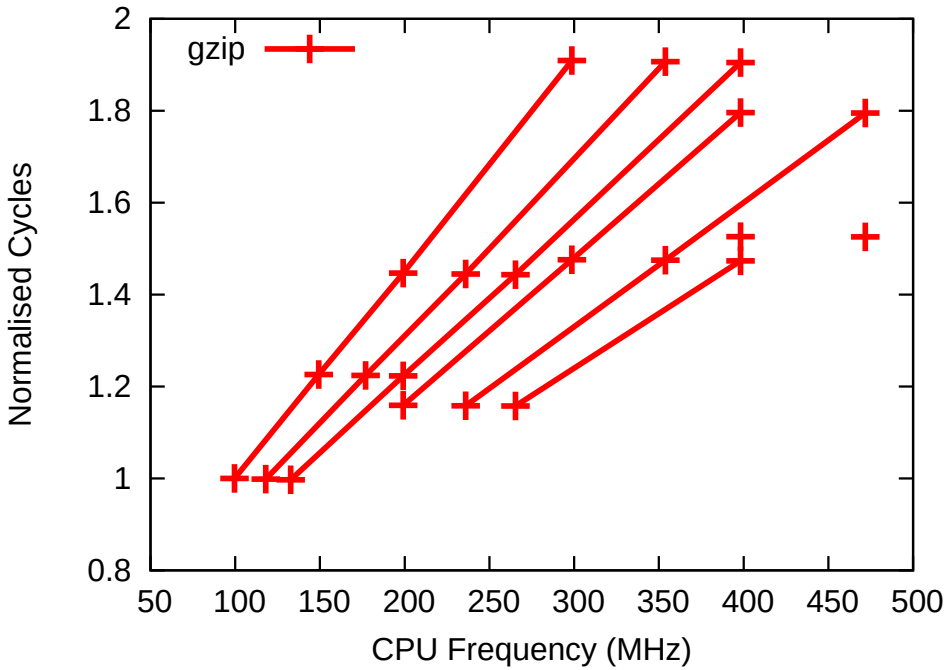

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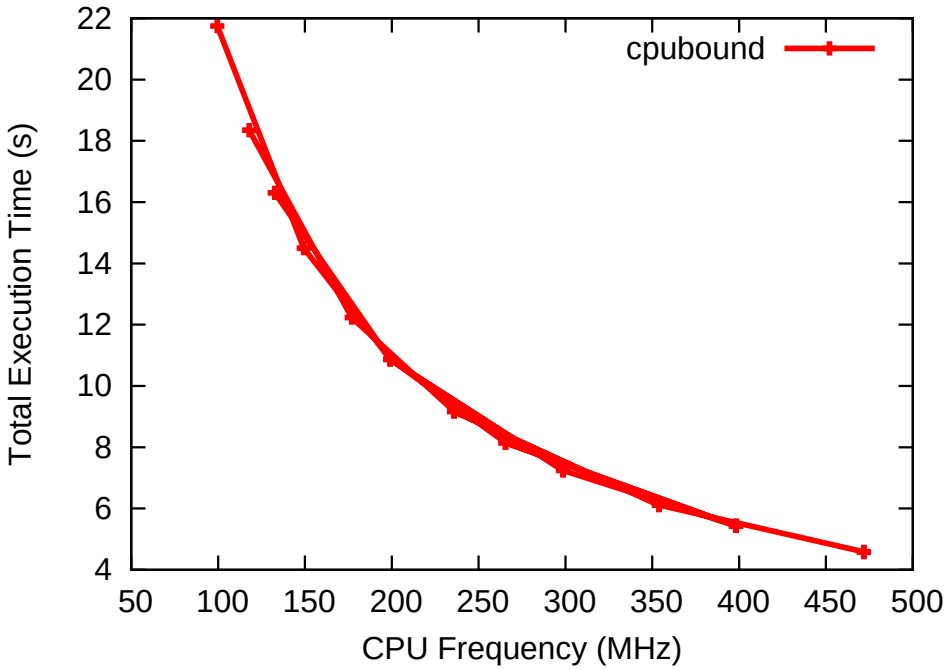
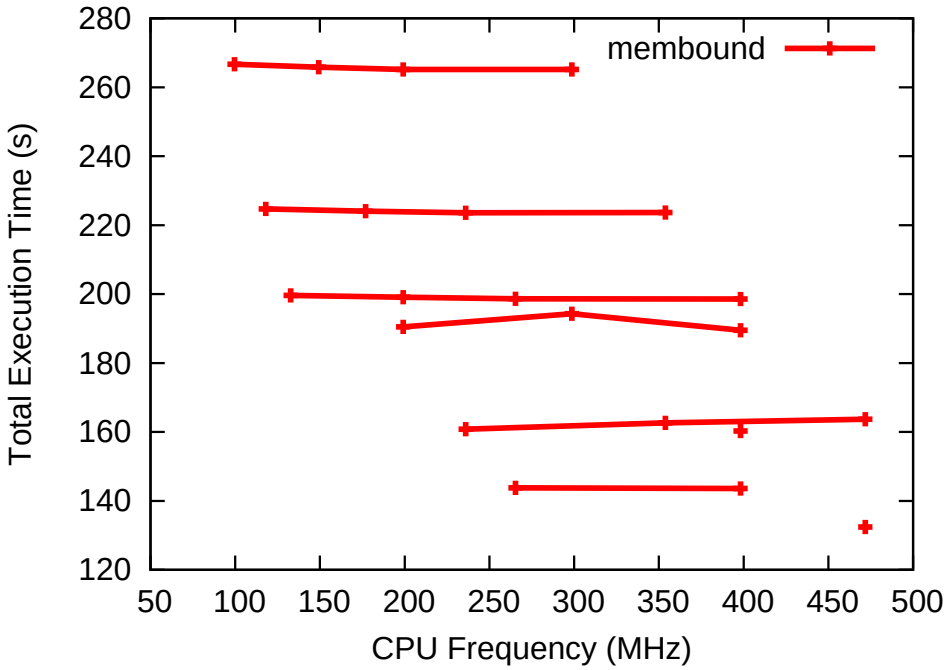
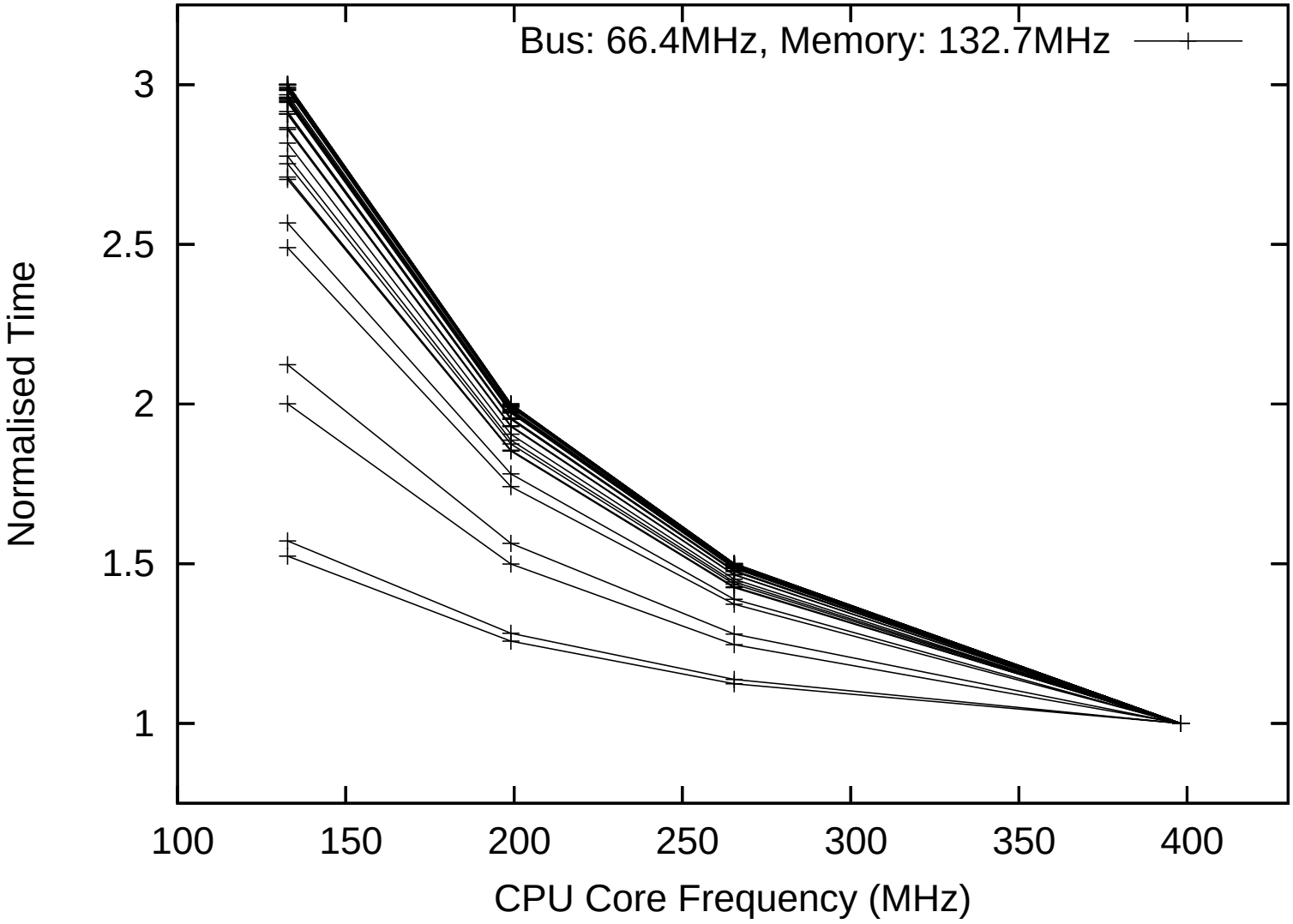




Real Program Behaviour



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  ➜ in modern processors static power is starting to dominate!
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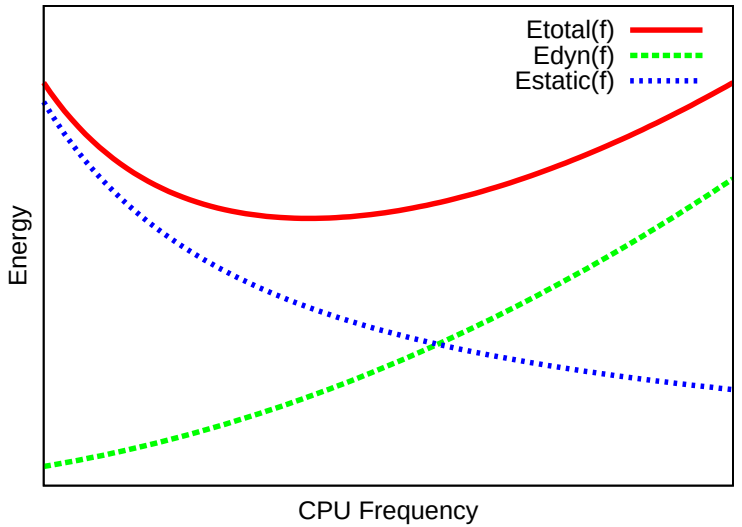

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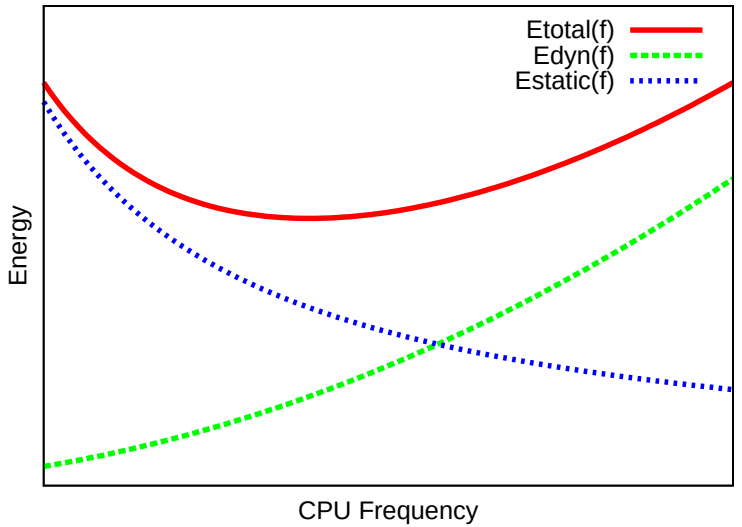
- Static *power* is independent of frequency
  - ➜ static *energy* is proportional to execution time!
- Hence, with increasing core frequency:
  - ➜ dynamic energy decreases
  - ➜ static energy increases
  - ➜ optimal frequency depends on relative size of static and dynamic power
  - ➜ lowest energy may be at intermediate frequency!



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- Minimising energy with DVFS requires:
  - ➜ prediction of *performance* (execution time) under DVFS
  - ➜ prediction of *power consumption* under DVFS
- Needs to happen in real time if *a-priori* characterisation is infeasible
  - ➜ can use performance counters (WB02)
  - ➜ needs to be done with low overhead

Realistic Execution Time Model

$$T = \frac{C_{cpu}}{f_{cpu}} + \frac{C_{bus}}{f_{bus}} + \frac{C_{mem}}{f_{mem}} + \frac{C_{io}}{f_{io}} + \cdots$$

- C_x represents the number of clock cycles for f_x.
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C_x: characterise online using performance counters

$$\begin{aligned} C_{bus} &= \alpha_1 PMC_1 + \alpha_2 PMC_2 + \ldots \\ C_{mem} &= \beta_1 PMC_1 + \beta_2 PMC_2 + \ldots \end{aligned}$$

(C_{cpu} inferred from the other results)

Realistic Execution Time Model

Estimating C_{cpu}:

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Realistic Execution Time Model

Estimating C_{cpu}:

- ➜ C_{cpu} is difficult to estimate using performance counters alone
- ➜ But...

$$C_{cpu} = C_{tot} - \frac{f_{cpu}}{f_{bus}} C_{bus} - \frac{f_{cpu}}{f_{mem}} C_{mem} + \cdots$$

- ➜ If we can measure cycles, we can estimate C_{cpu}.
- ➜ Or... If we can estimate the off-chip cycles, we can calculate the on-chip cycles.

Evaluation

The data:

- ➜ Typical embedded platform (PLEB 2, XScale based)
- ➜ Cycle counter, 2 performance counters, 13 events
- ➜ 22 frequency setpoints with different f_{cpu}, f_{bus} and f_{mem}
- ➜ 37 benchmarks run to completion at each setpoint for all frequency settings
- ➜ All performance counter events were measured end-to-end for each benchmark/frequency
- ➜ Benchmarks were partitioned for calibration and validation
- ➜ Measurements: Cycles, Frequencies, Performance counters

Evaluation

Which counters are the best to use?

Per workload:

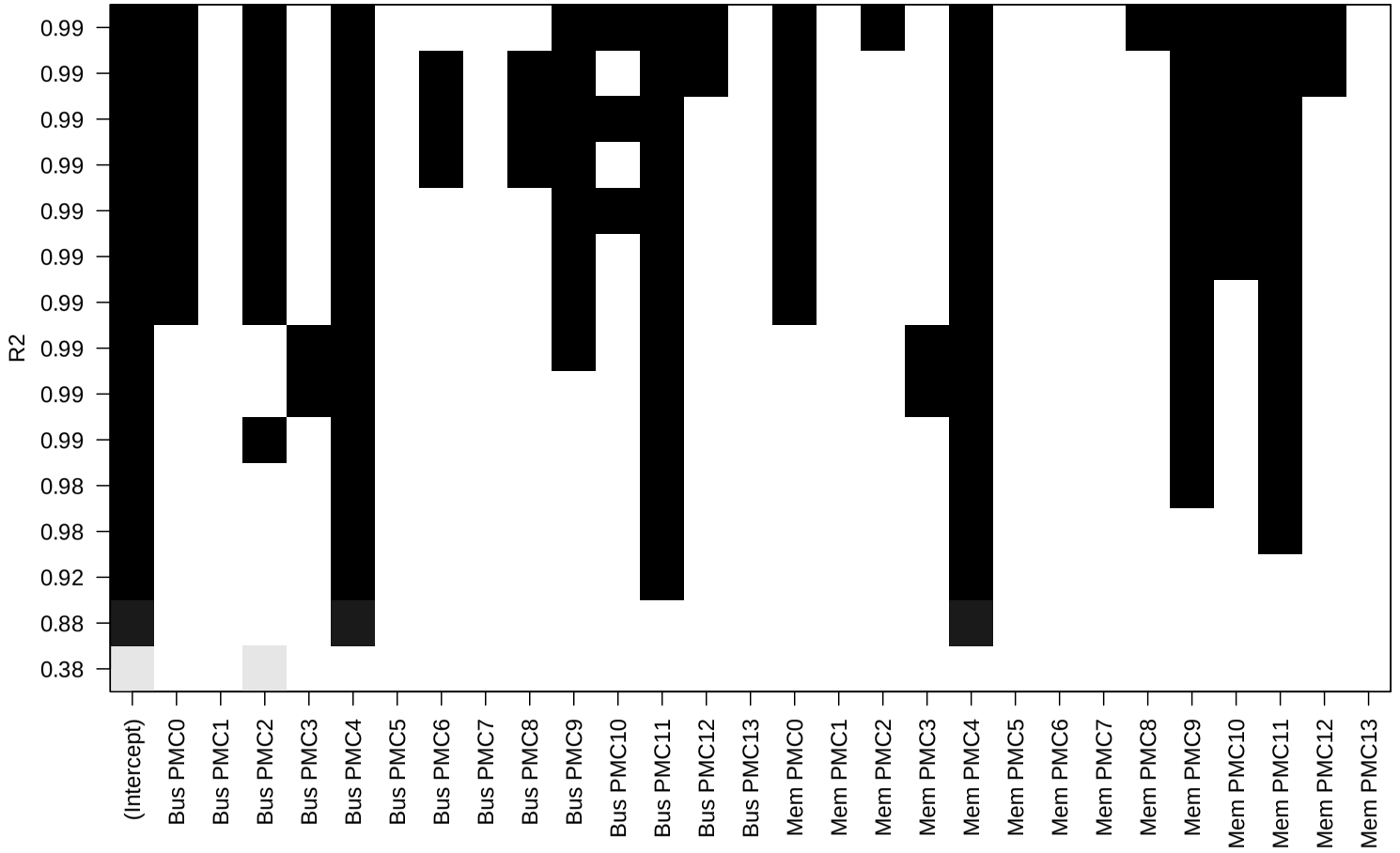
$$T = \frac{C_{cpu}}{f_{cpu}} + \frac{C_{bus}}{f_{bus}} + \frac{C_{mem}}{f_{mem}} + \frac{C_{io}}{f_{io}} + \ldots$$

Per platform:

$$C_{bus} = \alpha_1 PMC_1 + \alpha_2 PMC_2 + \ldots$$
$$C_{mem} = \beta_1 PMC_1 + \beta_2 PMC_2 + \ldots$$

- ➜ Fit for each benchmark for the average PMC_x
- ➜ Exhaustive parameter selection based on bic or R^2.

Picking Performance Counters



➜ Best correlation of power and PMC readings for different number of counters

USING THE MODEL

Making predictions:

How long would it have taken to run at XX MHz?

$$C'_{tot} = C_{tot} - \frac{f_{cpu}}{f_{bus}} C_{bus} - \frac{f_{cpu}}{f_{mem}} C_{mem} + \frac{f'_{cpu}}{f'_{bus}} C_{bus} + \frac{f'_{cpu}}{f'_{mem}} C_{mem}$$

Errors:

- ➜ Predicting the performance at the maximum frequency
- ➜ 2-parameter: avg 1.7%, max 7%
- ➜ CPU frequency only: avg 10%, max 36%

USING THE MODEL

Relative performance:

➜ Often we want a normalised performance (e.g. 50% of maximum).

$$s = \frac{t^{max}}{t'} = \frac{f'_{cpu}}{f^{max}_{cpu}} \times \frac{C^{max}_{tot}}{C'_{tot}}$$

This is a linear equation in terms of the PMCs

Power/Energy model

Power/Energy model basics:

For our system:

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- ➜ *Events* each use an amount of energy
- ➜ An event may use energy in more than one voltage domain

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$$E_{events} = V_{cpu}^2(\alpha_0 PMC_0 + \cdots + \alpha_m PMC_m) + \beta_0 PMC_0 + \cdots + \beta_m PMC_m$$

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$$E_{freqs} = V_{cpu}^2(\gamma_1 f_{cpu} + \gamma_2 f_{bus} + \gamma_3 f_{mem})\Delta t + (\gamma_4 f_{cpu} + \gamma_5 f_{bus} + \gamma_6 f_{mem})\Delta t$$

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- ➜ Constant IO power for the benchmarks tested.

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$$E_{static} = P_{static}\Delta t$$

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For our system:

$$E_{events} = V_{cpu}^2(\alpha_0 PMC_0 + \cdots + \alpha_m PMC_m) + \beta_0 PMC_0 + \cdots + \beta_m PMC_m$$

$$E_{freqs} = V_{cpu}^2(\gamma_1 f_{cpu} + \gamma_2 f_{bus} + \gamma_3 f_{mem})\Delta t + (\gamma_4 f_{cpu} + \gamma_5 f_{bus} + \gamma_6 f_{mem})\Delta t$$

$$E_{static} = P_{static}\Delta t$$

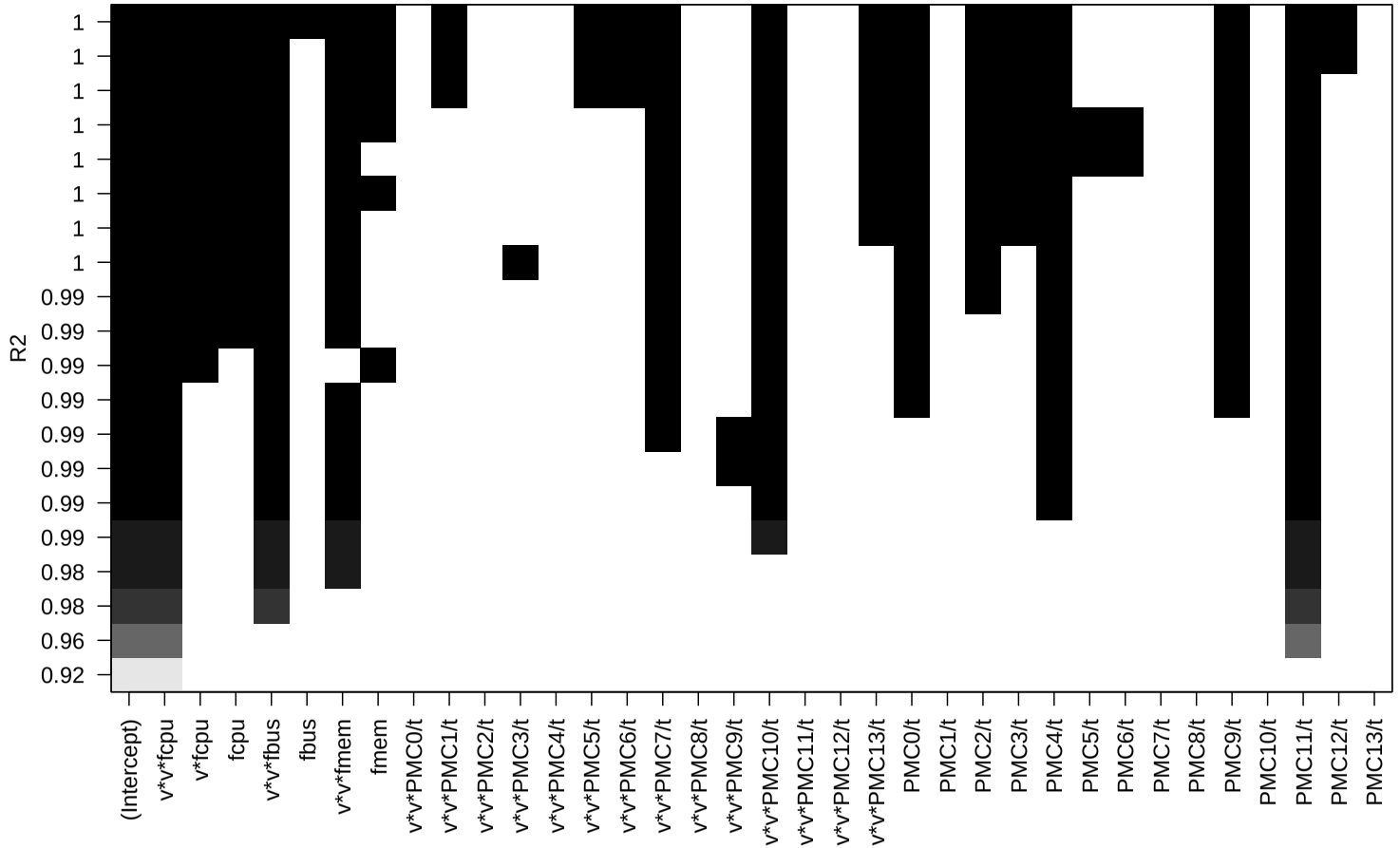
Time is essential for either power or energy estimation

Power/Energy model

The Data:

- Same as ETM data
- End-to-end energy measured using a shunt resistor
- Measurements triggered using a GPIO
- Each workload sample is used to predict the power for every other sample
- Frequency and voltage are varied independently

Power/Energy model



Power/Energy model

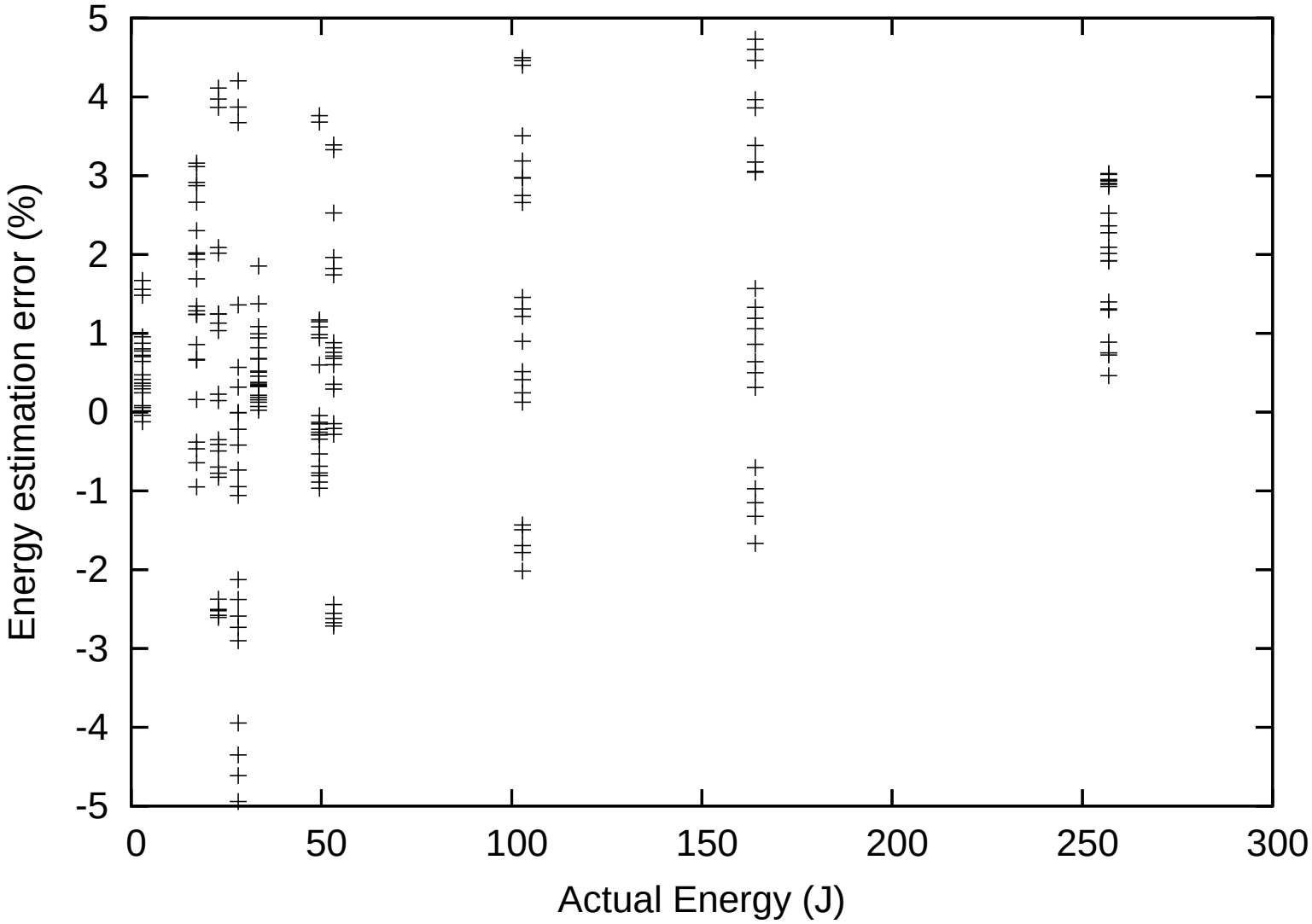
Power error data (using a measured run-time):

Counters	Param.	R^2	Max Err (%)	Avg Err (%)
1	4	0.9836	7.46	2.14
2	5	0.9871	6.94	2.31
3	6	0.9904	4.85	1.26
4	7	0.9922	3.78	1.16
5	8	0.993	3.68	0.92
6	9	0.9938	2.94	0.89
6	11	0.9947	2.75	0.77

Energy error data (estimated run-time — four counters):

➜ Max: 4.9%, Avg: 1.5%

Power/Energy model



Using the models

Sound approach:

- Determine appropriate PMC set and weights via systematic process
  - once per platform
- Use these to predict performance and power for actual load at run time
- Context-switch DVFS settings

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Using these results:

- Thread-level DVFS.
- Identify appropriate frequency choices
- $\boldsymbol{Energy \cdot Delay}$
- Sleep mode vs. DVFS trade-offs

USING THE MODELS

Performance predictions at run-time:

- A toy system: frequency scaling in Linux
- Measures the performance counters after each time slice
- Predicts the performance at all of the other setpoints for that time-slice
- Assuming temporal locality, chooses the setpoint with the closest to a chosen performance
- Error: avg 1.9%, max 7%

Not useful in itself, but demonstrates the model