CPU performance increases are slowing

Multiprocessor System

A single CPU can only go so fast
- Idea: Use more than one CPU to improve performance
- Assumes
  - Workload can be parallelised
  - Workload is not I/O-bound or memory-bound

Amdahl’s Law

Given:
- Parallelisable fraction \( P \)
- Number of processors \( N \)
- Speed up \( S \)
\[
S(N) = \frac{1}{(1 - P) + \frac{P}{N}}
\]
\[
S(\infty) = \frac{1}{1 - P}
\]

Parallel computing takeaway:
- Useful for small numbers of CPUs (\( N \))
- Or high values of \( P \)
  - Aim for high \( P \) values by design

Types of Multiprocessors (MPs)

Classic symmetric multiprocessor (SMP)
- Uniform Memory Access
  - Access to all memory occurs at the same speed for all processors.
- Processors with local caches
  - Separate cache hierarchy
  - Cache coherency issues
**Cache Coherency**

What happens if one CPU writes to address 0x1234 (and it is stored in its cache) and another CPU reads from the same address (and gets what is in its cache)?

- Can be thought of as managing replication and migration of data between CPUs
- Note: The unit of replication and consistency is the cache line

**Problematic Example**

```plaintext
s = 1
if b == 0 then {
    /* critical section */
    s = 0
} else {
    ...
}
```

- For classic SMP a hardware solution is used
- Write-through caches
  - Each CPU cache snoops bus activity to invalidate stale lines
  - Reduces cache effectiveness – all writes go out to the bus.
    - Longer write latency
    - Reduced bandwidth

**Memory Model: Sequential Consistency**

"The result of any execution is the same as if the operations of all the processors were executed in some sequential order, and the operations of each individual processor appear in this sequence in the order specified by its program." [Lamport, 1979]

**With sequential consistency**

```plaintext
a = 1
if b == 0 then {
    /* critical section */
    a = 0
} else {
    ...
}
```

**Types of Multiprocessors (MPs)**

**NUMA MP**

- Non-uniform memory access
  - Access to some parts of memory is faster for some processors than other parts of memory
  - Provides high-local bandwidth and reduces bus contention
- Assuming locality of access
How is such a machine kept consistent?

Snooping caches assume
- write-through caches
- cheap "broadcast" to all CPUs

Many alternative cache coherency protocols
- They improve performance by tabling above assumptions
  - We'll examine MESI (four state)
    - Optimisations exist (MOESI, MESIF)
    - ‘Memory bus’ becomes message passing system between caches

Example Coherence Protocol MESI

Each cache line is in one of four states

Invalid (I)
- This state indicates that the addressed line is not resident in the cache and/or any data contained is considered not useful.

Exclusive (E)
- The addressed line is in this cache only.
- The data in this line is consistent with system memory.

Shared (S)
- The addressed line is valid in the cache and in at least one other cache.
- A shared line is always consistent with system memory. That is, the shared state is shared-unmodified; there is no shared-modified state.

Modified (M)
- The line is valid in the cache and in only this cache.
- The line is modified with respect to system memory—that is, the modified data in the line has not been written back to memory.

Example

Cache
CPU
Cache
CPU
Main Memory

 MESI (with snooping/broadcast)

Events
- RH = Read hit
- RMS = Read miss, shared
- RME = Read miss, exclusive
- WH = Write hit
- WM = Write miss
- SHR = Snoop hit on read
- SHI = Snoop hit on invalidate
- LRU = LRU replacement

Bus Transactions
- Push = Write-cache line back to memory
- Invalidate = Broadcast invalidate
- Read = Read cache line from memory

Performance improvement via write-back caching
- Less bus traffic

Directory-based coherence
Each memory block has a home node
- Home node keeps directory of
  - caches that have a copy
- E.g., a bitmap of processes per cache line

Pro
- Invalidation update messages can be directed explicitly
  - No longer rely on broadcast/snooping

Con
- Requires more storage to keep directory
  - E.g., each 256 bits of memory (cache line) requires 32 bits (processor mask) of directory

Example
Summary

Hardware-based cache coherency:
• Provide a consistent view of memory across the machine.
• Read will get the result of the last write to the memory hierarchy

Memory Models: Strong Ordering

Sequential consistency
- The result of any execution is the same as if the operations of all the processors were executed in some sequential order, and the operations of each individual processor appear in this sequence in the order specified by its program.

Traditionally used by many architectures
Assume X = Y = 0 initially

<table>
<thead>
<tr>
<th>CPU 0</th>
<th>CPU 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>store 1, X</td>
<td>store 1, X</td>
</tr>
<tr>
<td>load r2, Y</td>
<td>load r2, X</td>
</tr>
<tr>
<td>X=1, Y=0</td>
<td>X=1, Y=0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CPU 0</th>
<th>CPU 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>store 1, Y</td>
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<td>load r2, X</td>
</tr>
<tr>
<td>store 1, Y</td>
<td>store 1, Y</td>
</tr>
<tr>
<td>load r2, X</td>
<td>load r2, X</td>
</tr>
<tr>
<td>X=0, Y=1</td>
<td>X=1, Y=1</td>
</tr>
</tbody>
</table>

Potential interleavings

At least one CPU must load the other's new value
- Forbidden result: X=0, Y=0

Realistic Memory Models

Modern hardware features can interfere with store order:
• Write buffer (or store buffer or write-behind buffer)
• Instruction reordering (out-of-order execution)
• Superscalar execution and pipelining

Each CPU/core keeps its own execution consistent, but how is it viewed by others?

Write-buffers and SMP

Stores go to write buffer to hide memory latency
• And cache invalidates

Loads read from write buffer if possible
Write-buffers and SMP

When the buffer eventually drains, what order does CPU1 see CPU0’s memory updates?

CPU 0
store r1, A
store r2, B
store r3, C

CPU 1

What happens in our example?

Total Store Ordering (e.g. x86)

Stores are guaranteed to occur in FIFO order

CPU 0
store 1, A
store 2, B
store 3, C

CPU 1 sees
A=1
B=2
C=3

Total Store Ordering (e.g. x86)

Stores are guaranteed to occur in FIFO order

CPU 0
store 1, X
load r2, Y

CPU 1
store 1, Y
load r2, X

What is the problem here?

Total Store Ordering (e.g. x86)

Stores are guaranteed to occur in FIFO order

CPU 0
store 1, X
load r2, Y

CPU 1
store 1, Y
load r2, X

Memory “fences”

Also called “barriers”
The provide a “fence” between instructions to prevent apparent re-ordering

Effectively, they drain the local CPU’s write-buffer before proceeding.
**Total Store Ordering**
Stores are guaranteed to occur in FIFO order

**Atomic operations?**
- Need hardware support, e.g.
  - atomic swap
  - test & set
  - load-linked + store-conditional
- Stall pipeline and drain (and/or bypass) write buffer
- Ensures addr1 held exclusively

**Partial Store Ordering (e.g. ARM MPcore)**
The barriers prevent preceding stores appearing after successive stores
- Note: Reality is a little more complex (read barriers, write barriers), but principle similar.
  - load r1, counter
  - add r1, r1, 1
  - store r1, counter
  - barrier
  - store zero, mutex
- Store to counter can overtake store to mutex
- i.e. update move outside the lock
- Need to use memory barrier
- Failure to do so will introduce subtle bugs:
  - Critical section "leaking" outside the lock

**MP Hardware Take Away**
Existing sync primitives (e.g. locks) will have appropriate fences/barriers in place
- In practice, correctly synchronised code can ignore memory model.
However, racey code, i.e. code that updates shared memory outside a lock (e.g. lock free algorithms) must use fences/barriers.
- You need a detailed understanding of the memory coherence model.
- Not easy, especially for partial store order (ARM).
Concurrency Observations

Locking primitives require exclusive access to the “lock”
- Care required to avoid excessive bus/interconnect traffic

Kernel Locking

Several CPUs can be executing kernel code concurrently.
Need mutual exclusion on shared kernel data.
Issues:
- Lock implementation
- Granularity of locking (i.e. parallelism)

Mutual Exclusion Techniques

Disabling interrupts (CLI — STI).
- Insufficient for multiprocessor systems.
Spin locks.
- Busy-waiting wastes cycles.
Lock objects (locks, semaphores).
- Flag (or a particular state) indicates object is locked.
- Manipulating lock requires mutual exclusion.

Hardware Provided Locking Primitives

int test_and_set(lock *);
int compare_and_swap(int c, int v, lock *);
int exchange(int v, lock *)
int atomic_inc(lock *)
v = load_linked(lock *) / bool
store_conditional(int, lock *)
- LL/SC can be used to implement all of the above

Spin locks

void lock (volatile lock_t *l) {
    while (test_and_set(l)) ;
}
void unlock (volatile lock_t *l) {
    *l = 0;
}
Busy waits. Good idea?

Spin Lock Busy-waits Until Lock Is Released

Stupid on uniprocessors, as nothing will change while spinning.
- Should release (block) thread on CPU immediately.
Maybe ok on SMPs: locker may execute on other CPU.
- Minimal overhead (if contention low).
- Should only spin for short time.
Generally restrict spin locking to:
- short critical sections,
- unlikely to (or preferably can’t) be contended by thread on same CPU.
  » local contention can be prevented
  » by design (per-CPU data structure)
  » by turning off interrupts
### Spinning versus Switching

- **Blocking and switching**
  - To another process takes time
  - Save context and restore another
  - Cache contains current process not new
  - TLB is similar to cache
  - Switching back when the lock is free encounters the same again

- **Spinning wastes CPU time directly**

  **Trade off**

  - If lock is held for less time than the overhead of switching to and back
  - It’s more efficient to spin

### Interrupt Disabling

Assume no local contention by design, is disabling interrupt important?

**Hint:** What happens if a lock holder is preempted (e.g., at end of its timeslice)?

All other processors spin until the lock holder is re-scheduled

### Alternative to spinning: Conditional Lock (TryLock)

```c
bool cond_lock (volatile lock t *l) {
    if (test_and_set(l))
        return FALSE; //couldn’t lock
    else
        return TRUE; //acquired lock
}
```

Can do useful work if fail to acquire lock.

**But** may not have much else to do.

**Livelock:** May never get lock!

### Another alternative to spinning.

```c
void mutex lock (volatile lock t *l) {
    while (1) {
        for (int i=0; i<MUTEX N; i++)
            if (!test_and_set(l))
                return;
        yield();
    }
}
```

Spins for limited time only

- Assumes enough for other CPU to exit critical section

Useful if critical section is shorter than N iterations.

**Starvation possible.**