

Scheduling Considerations for Voter Checking in TMR-MER Systems

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SRAM-based FPGAs deployed in space-based systems are susceptible to radiation-induced *Single Event Upsets* (SEUs). A common technique for dealing with SEUs is *Triple Modular Redundancy* (TMR) combined with *Module-based configuration memory Error Recovery* (MER) [1]. By triplicating components and voting on their outputs, TMR helps localize configuration memory errors, and by reconfiguring the faulty component, MER swiftly corrects the errors. TMR-MER systems utilize a *Reconfiguration Control Network* (RCN) to convey the status of the individual TMR component voters to a *Reconfiguration Controller* (RC), which determines whether configuration memory errors are present [2]. To determine whether any configuration memory upsets have occurred, TMR-MER systems typically check the voters of the TMR components in round-robin order. However, the order in which the voters of TMR components are checked has an inevitable impact on the overall system reliability. In our previous work, we developed methods for identifying the next component to check at run time based on the likelihood that it has failed since the last check [3]. In contrast, this paper reports on an off-line approach to determining a fixed voter checking sequence that maximizes system reliability.

Our work aims to enhance the system's error detection capabilities and raise overall system reliability by checking the voters of TMR components for module errors at different rates that are based on their susceptibility to errors. We outline an approach for computing the reliability of TMR-MER systems that consist of finitely many components assuming consecutive SEUs affect multiple modules of a TMR component [4]. Using the derived reliability models we demonstrate that the system reliability is improved when the more susceptible components are checked more frequently for the presence of configuration memory errors. We propose a genetic algorithm for finding a static voter checking schedule (so-called *Variable-Rate Voter Checking* (VRVC)) that maximizes TMR-MER system reliability.

We simulated a Xilinx Artix-7 XC7A200T device operating in Geostationary Equatorial Orbit (GEO) and at Low-Earth Orbit (LEO). The radiation levels at these orbits are expected to result in 2.66E-10 and 8.46E-12 upsets/bit/s respectively [4]. Fig. 1 shows that the *Mean Time To Failure* (MTTF) of TMR-MER systems is increased when VRVC is used instead of round robin to check voters. The improvements were found to be over 60%, 40% and 20% in simulations of systems consisting of 3–5, and 10 components ranging in size from 10,000 to

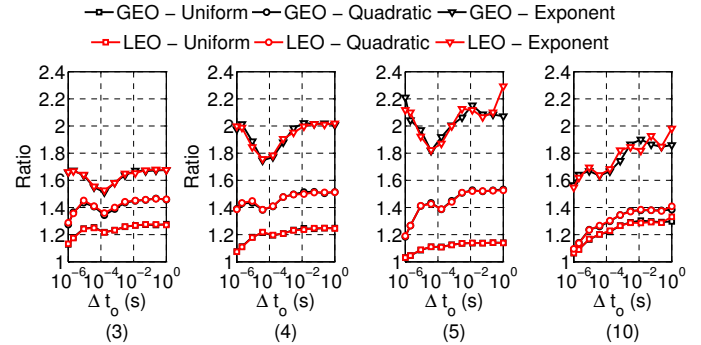


Fig. 1: Average ratios of MTTFs for VRVC to those for round robin for systems consisting of 3, 4, 5, and 10 components. Note that Δt_o denotes the time period between successive voter observations.

2,000,000 essential bits and assuming the number of essential bits for each component is exponentially, quadratically and uniformly distributed, respectively. Fig. 1 also shows that the ratios are almost independent of the upset rates expected in different orbits. Moreover, the power consumption of TMR-MER systems can be reduced without compromising system reliability by reducing the operating clock frequency of the RC. Finally, the results of fault injection testing demonstrated that the mean time to detect errors can be reduced by 30% when using VRVC instead of round robin [4].

We assert that any FPGA-based TMR-MER system that uses an RCN to provide random access to component voters can benefit from using VRVC. The benefits become more significant as the checking frequency decreases or as the disparity in the number of essential bits per TMR component increases [4].

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