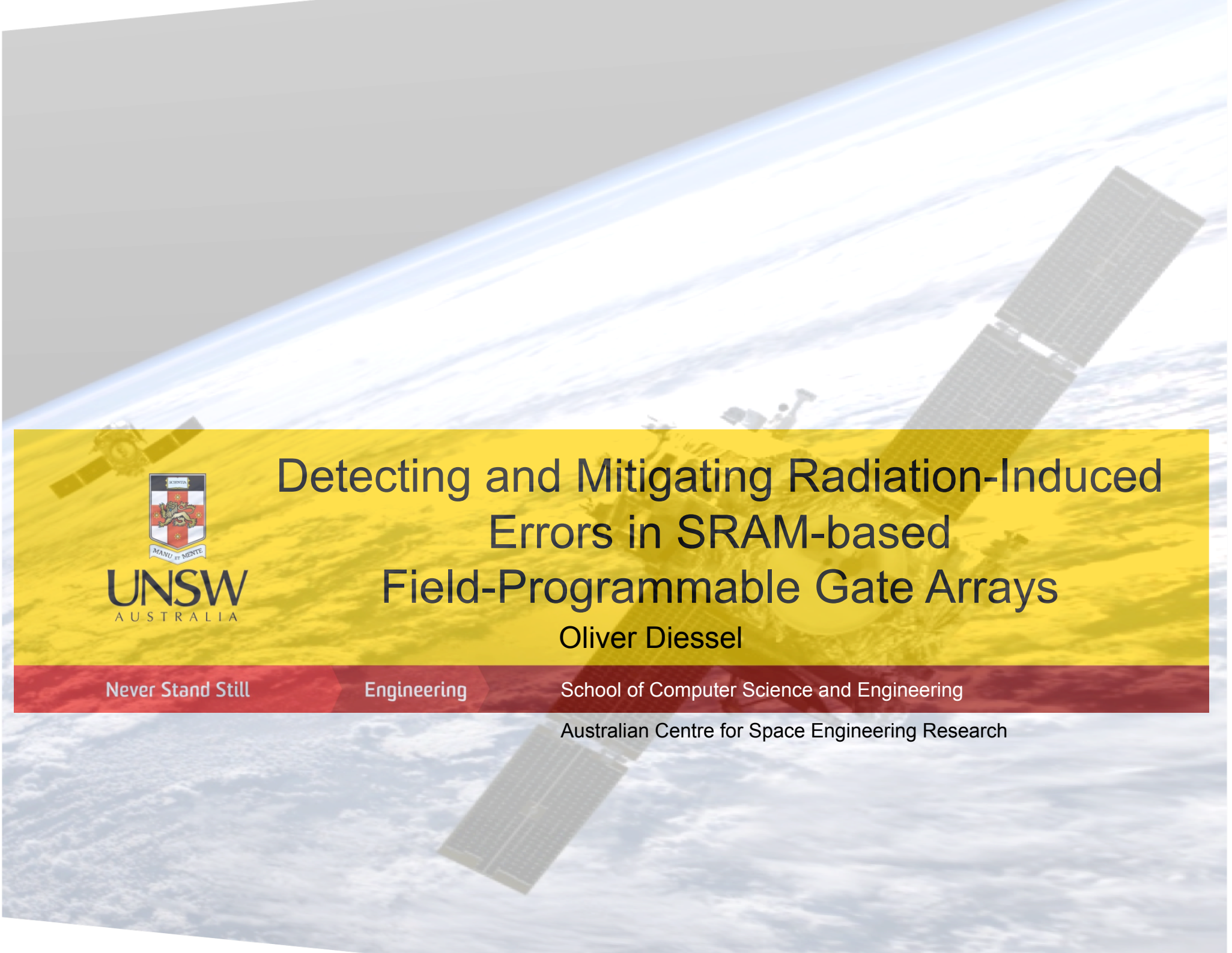

Detecting and Mitigating Radiation-Induced Errors in SRAM-based Field-Programmable Gate Arrays

Oliver Diessel

UNSW AUSTRALIA

Never Stand Still | Engineering | School of Computer Science and Engineering

Australian Centre for Space Engineering Research

Talk outline

- Explain why radiation-induced errors are a serious threat to FPGA-based systems
- Describe state-of-the-art for detecting and mitigating SEUs in commercial FPGAs
- Outline current work in testing & evaluating competing solutions
- Forecast the future

Why am I talking about SEU mitigation?

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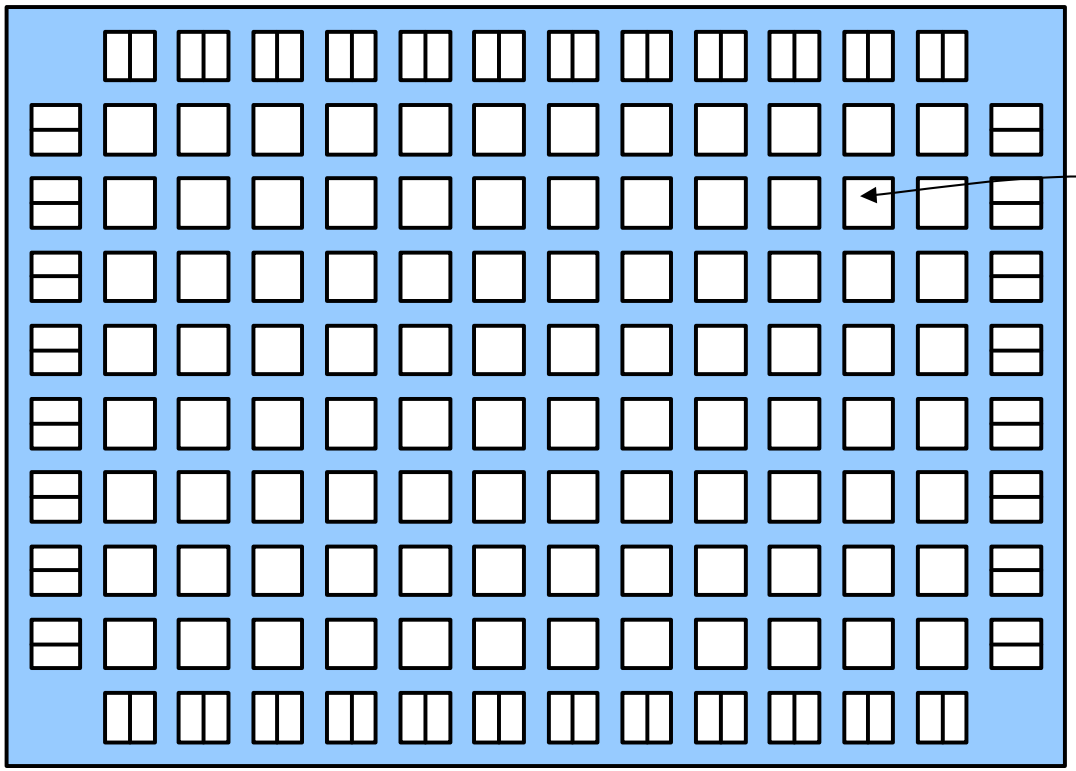
What's inside an FPGA?



Logic Blocks

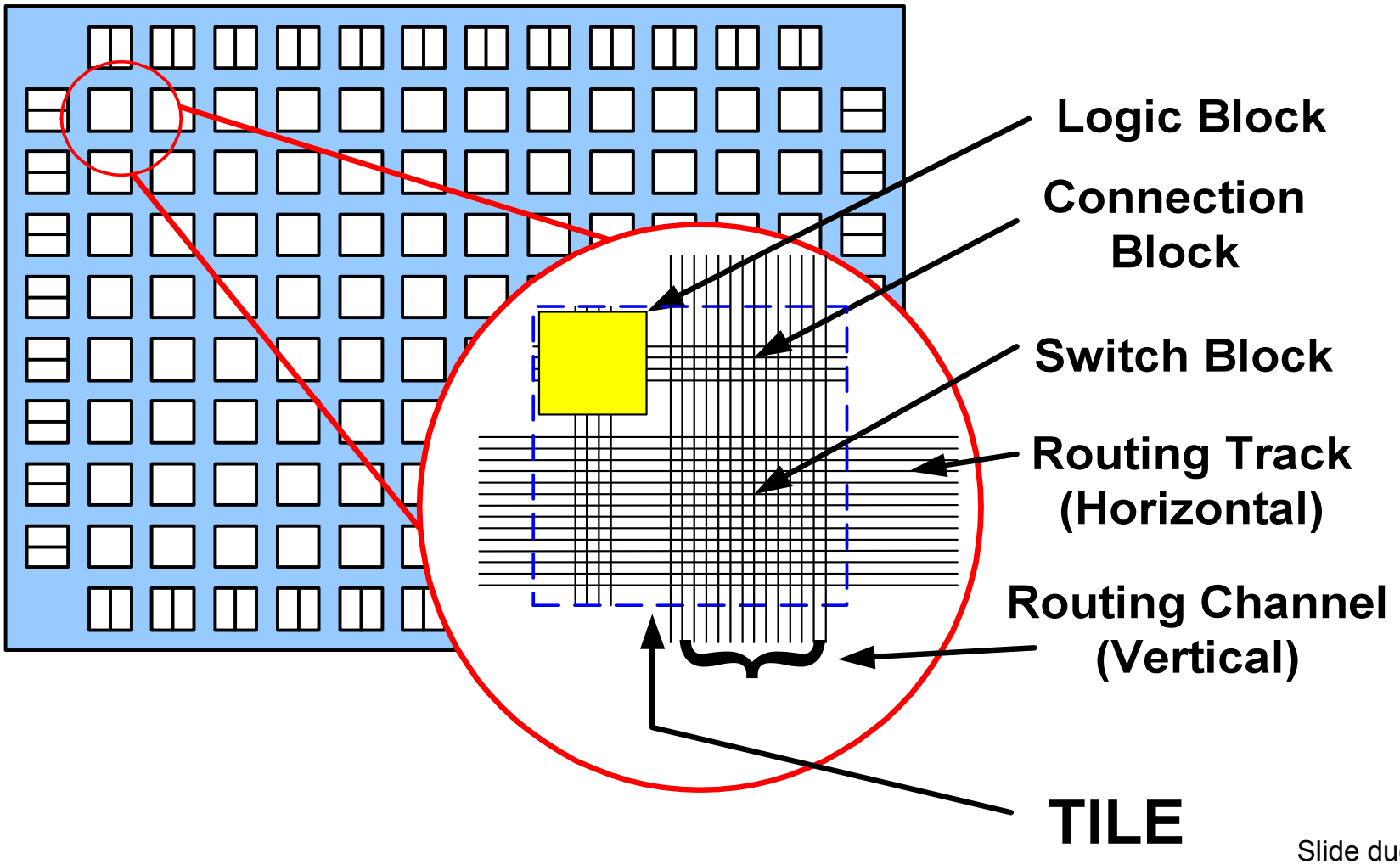
- comprise lookup tables and flip-flops

Altera: LABs

Xilinx: CLBs

Slide due to Steve Wilton

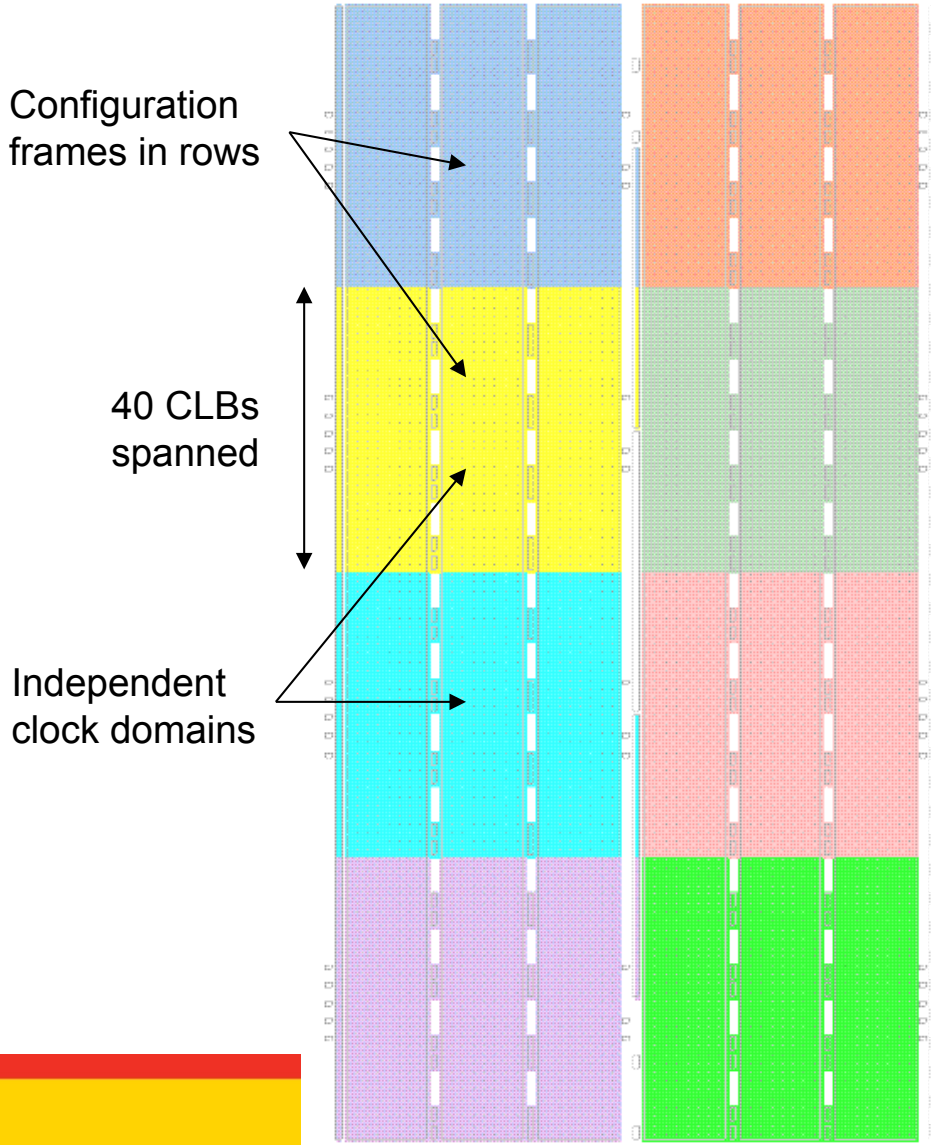
What's inside an FPGA?



Slide due to Steve Wilton

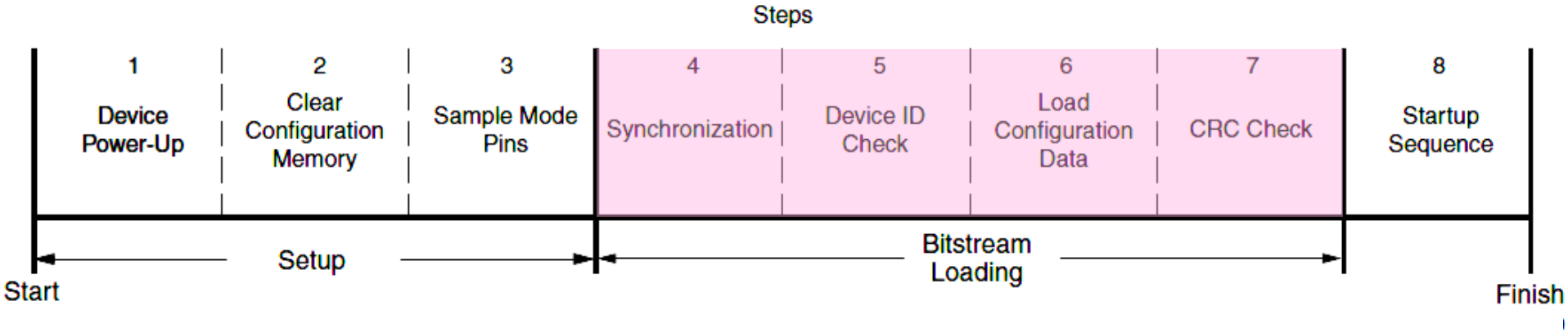
FPGA configuration memory architecture

- Organized into frames:
  - 101x 32-bit words for Xilinx-7
- The configuration memory of an FPGA comprises
  - CMOS configuration latch settings to determine all routes
  - Settings to configure each LUT
  - Contents of embedded memory blocks
  - Configuration of DSP slices clock managers, PLLs, ADCs, SerDes blocks, high-speed transceivers, IO blocks, etc.



FPGA configuration

- FPGAs are configured by loading a bitstream to the device



- Bitstream organisation:

  <preamble><start address><num frames><frame content>…<postamble>

- Bitstream size varies:
  - Artix-7 7A15T: ~17 Mbits (smallest Xilinx 7-series device)
  - Virtex-7 7VX1140T: ~385 Mbits (largest Xilinx 7-series device)
- **Complete** versus **Partial** Bitstream
- **Writing** versus **Reading** frame contents

COTS FPGAs in Space

- Space-based systems play increasingly important roles in the efficient functioning of modern societies
- Growing international interest in the development of space missions based on low-cost nano-/microsatellites e.g. CubeSats, demands new approaches to the design of reliable, low-cost, reconfigurable digital processing platforms
- Commercial, off-the-shelf SRAM-based FPGAs are ideally suited to meeting these demands

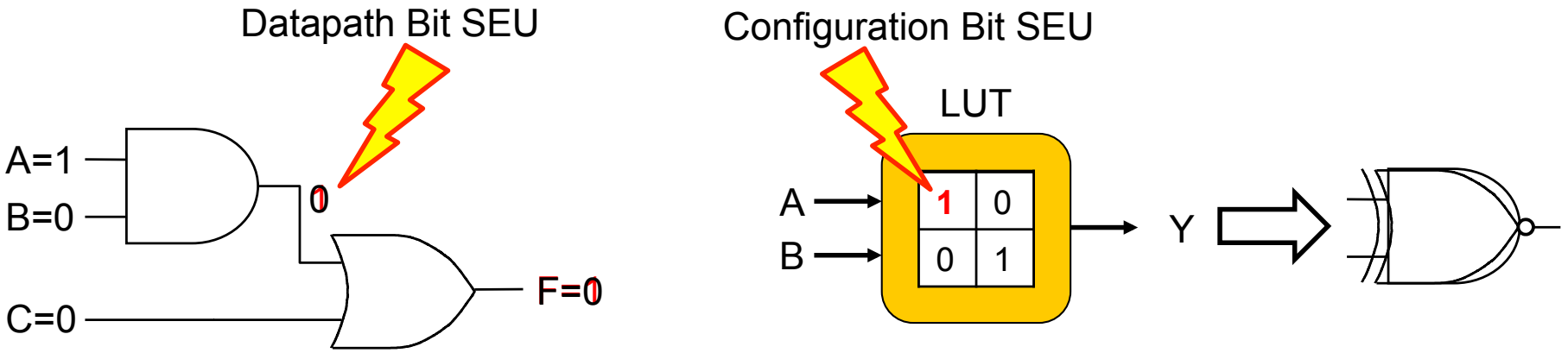
Space-based applications for FPGAs

A mixture of control-oriented and computationally intensive tasks:

- On-board computer – control; interfacing; real time – all low power
- Communications – baseband; encryption; decryption
- Flight control
- Global positioning
- Image capture and processing; pre-filtering; compression
- Synthetic aperture radar

FPGA susceptability to SEUs

- BUT…FPGAs are particularly susceptible to radiation-induced Single Event Upsets (SEUs)
  - Deposited charge causes a change of state in dynamic circuit elements
  - Affects both datapath and configuration memory
    - Can corrupt any configurable resource
    - Routing, logic & memory particularly susceptible



FPGA susceptability to SEUs

- SEU occurrence increases with orbit radius

Orbit	SEUs/day	MTTU (s)
LEO (560 km)	4.09	2.11×10^4
Polar (833 km)	1.49×10^4	5.81
GPS (20,200 km)	5.46×10^4	1.58
Geosynchronous (36,000 km)	6.2×10^4	1.39

Predictions for Virtex-4 (XC4VLX200) [Engel et al., 2006]

FPGA susceptability to SEUs

- SEUs have more significant impact as transistor sizes shrink

Device Family	Technology Node	Total Events	1-Bit Events	2-Bit Events	3-Bit Events	4-Bit Events
Virtex	250 nm	241,166	241,070 (99.996%)	96 (0.004%)	0 (0%)	0 (0%)
Virtex-II	150 nm	541,823	523,280 (98.42%)	6,293 (1.16%)	56 (0.01%)	3 (0.001%)
Virtex-II Pro	130 nm	10,430	10,292 (98.68%)	136 (1.30%)	2 (0.02%)	0 (0%)
Virtex-4	90 nm	152,577	147,902 (96.44%)	4,567 (2.99%)	78 (0.05%)	8 (0.005%)

Event distribution due to proton radiation @63.3 MeV [Quinn et al., 2005]

Dealing with soft errors

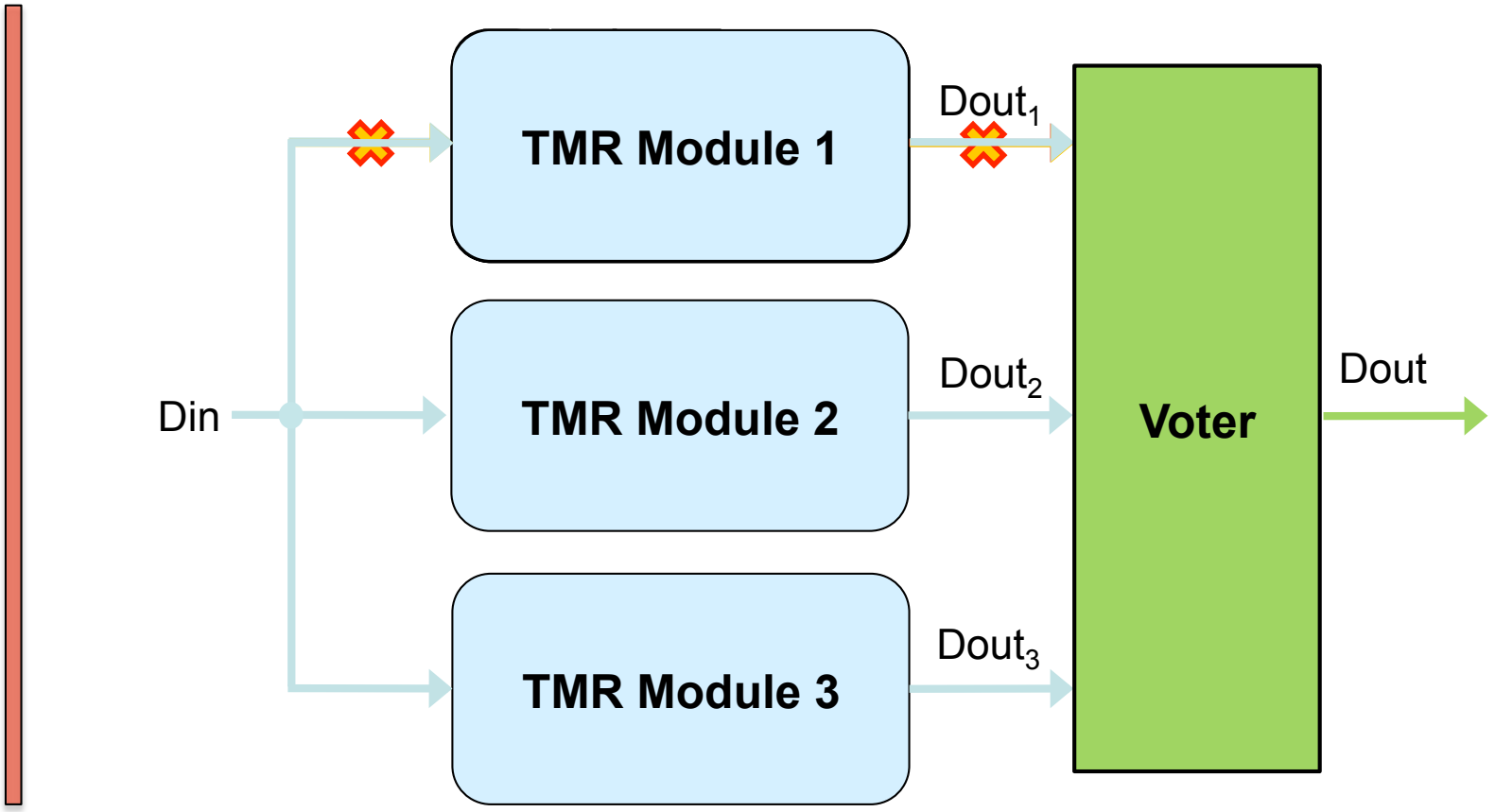
1. Radiation-hardened FPGAs
   - Expensive, small, superseded technology, restricted
2. Error Detection And Correction (EDAC)
   - Limited capacity to detect and correct errors in the user circuitry
   - Limited capacity to assist in detecting configuration memory errors
3. Triple Modular Redundancy (TMR)
   - Effective masking of errors that affect a single module
   - Capable of assisting in detecting configuration memory errors
4. Reconfiguration
   a. Complete
      - Corrects all configuration memory errors
   b. Partial
      - Limited capacity to assist with correcting configuration memory errors

Dealing with soft errors

- Critical systems that need to be highly available & reliable use Triple Modular Redundancy to deal with transient errors in the datapath
- Soft errors can also affect configuration memory
  - Symptoms can be similar to a permanent fault
  - These errors can be eliminated by reconfiguration
    - **Scrubbing**
      - Periodic refresh of entire configuration memory
      - Slow and costly in terms of energy (transfer several MB)
    - **Modular reconfiguration**
      - Reconfigure the module in which a fault is present
      - Useful when quicker response or higher availability is desired
      - More complex to implement

SEU mitigation in FPGAs

- Triple Modular Redundancy (TMR)
  - Eliminating configuration errors by scrubbing
  - Or by dynamic modular reconfiguration



Scrubbing

- Uses special IP: SEM Controller
- Repeat:
  - Read each configuration frame
  - Check ECC of frame
  - If single error found, then correct error and restart scan
  - Check CRC

Modular Reconfiguration

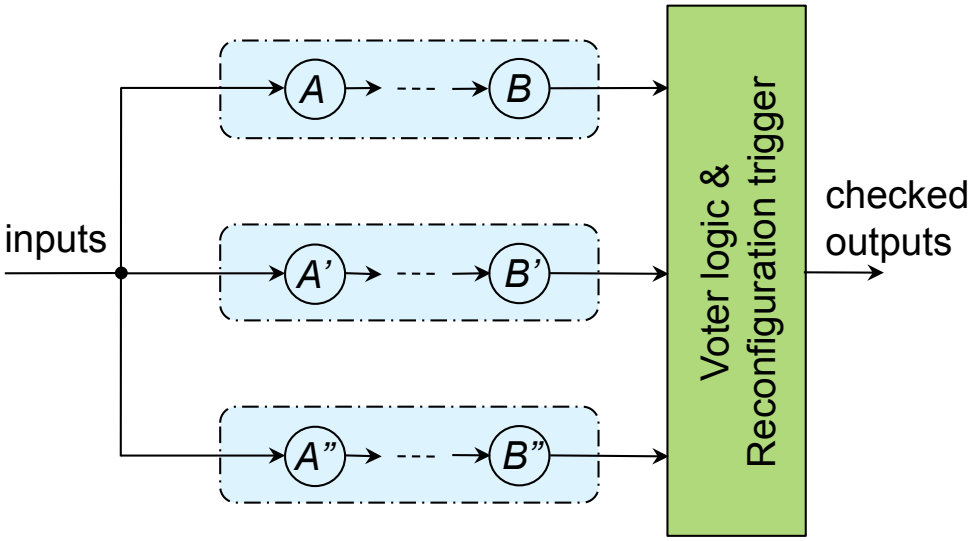
- Compose design of "reconfigurable partitions"
- Detect an error in a module via the TMR voter
  - Raise request to reconfigure module
  - Fetch a "partial bitstream" for the module from off-chip
  - Reload partial bitstream to correct configuration memory error

For Both Methods

- Need to decide how to resynchronize user logic
- Need to rely on complete reconfiguration when the method fails to correct the errors present

Acyclic circuits

- Simplest case:
  - Pipeline or linear filter
  - Streamed data

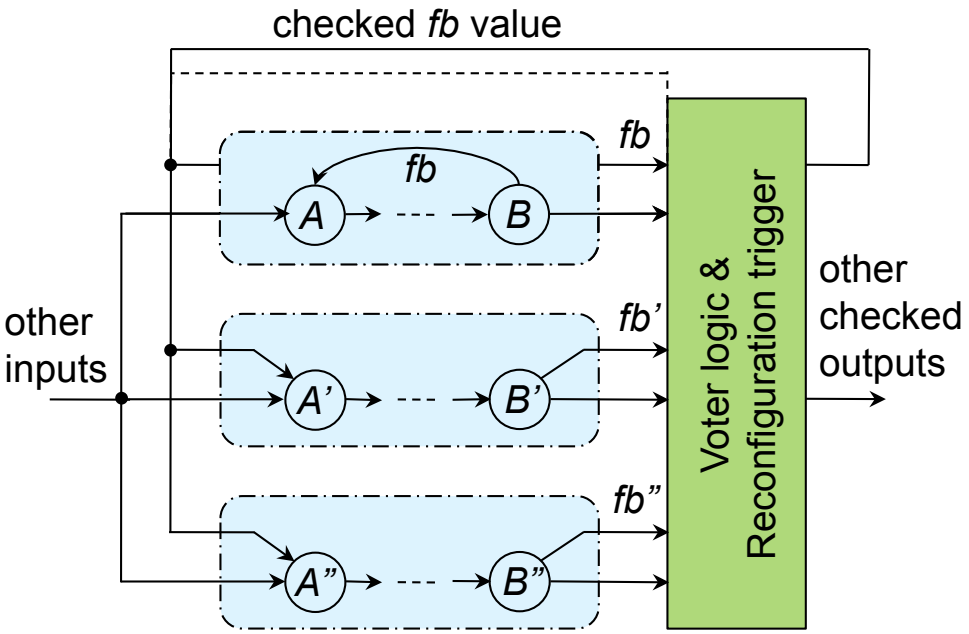


- Represent as acyclic DFG
  - Node = Op [+ Reg]
  - Edge = Data transfer
- > *k* successive errors trigger reconfiguration of faulty module
- Time to detect fault:

  $t_{D\_MAX} \leq N$ clock cycles
- Time to recover from fault:

  $\leq 2t_{D\_MAX} + t_R$ clock cycles

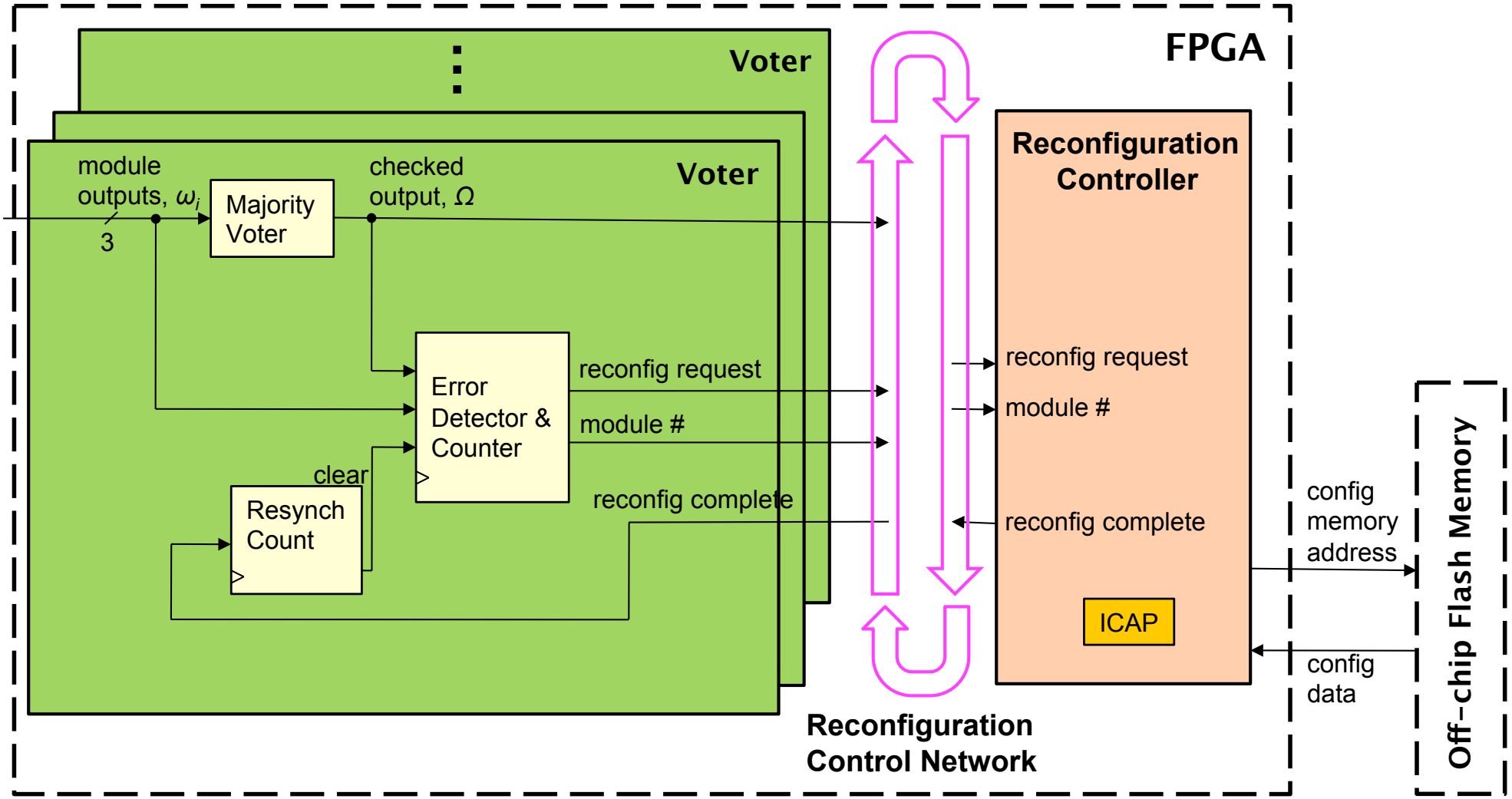
Cyclic circuits



- The cause of persistent faults in cyclic components cannot be determined
- The correct state cannot be set by presenting new inputs to the circuit

⇒ Cut feedback edges & vote on them; recycle *fb* as an input to an otherwise acyclic component

Reconfiguration control



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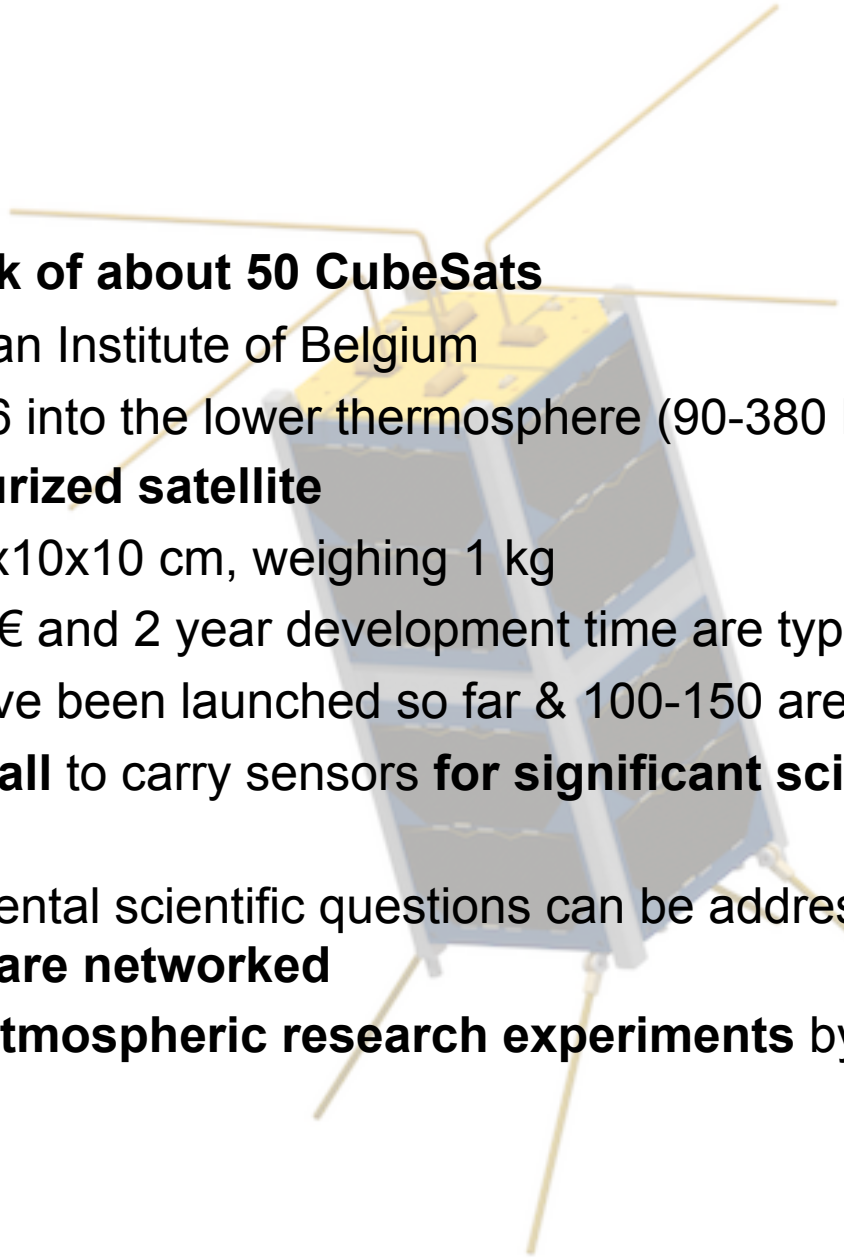
QB50 Project



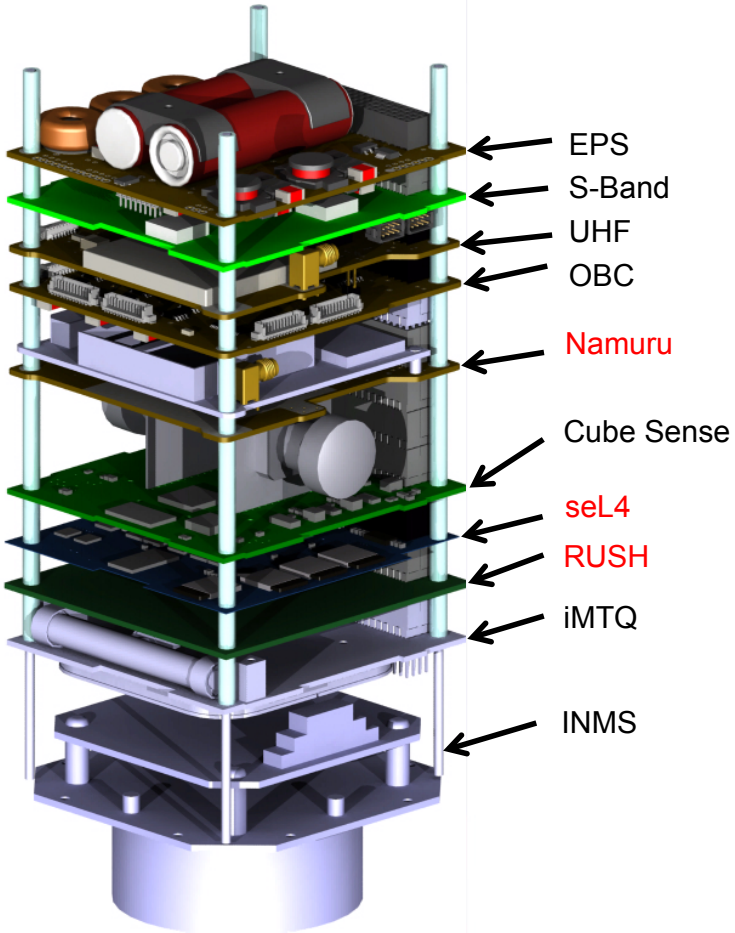
- **International network of about 50 CubeSats**
  - Led by Von Karman Institute of Belgium
  - launch by 12/2016 into the lower thermosphere (90-380 km orbit)
- **CubeSat is a miniaturized satellite**
  - 1U measuring 10x10x10 cm, weighing 1 kg
  - Costs of 50-100 k€ and 2 year development time are typical
  - ≈50 CubeSats have been launched so far & 100-150 are planned
- A **CubeSat is too small** to carry sensors **for significant scientific research**
  - However, fundamental scientific questions can be addressed **when many CubeSats are networked**
- QB50 will conduct 3 **atmospheric research experiments** by networking 40 × 2U CubeSats

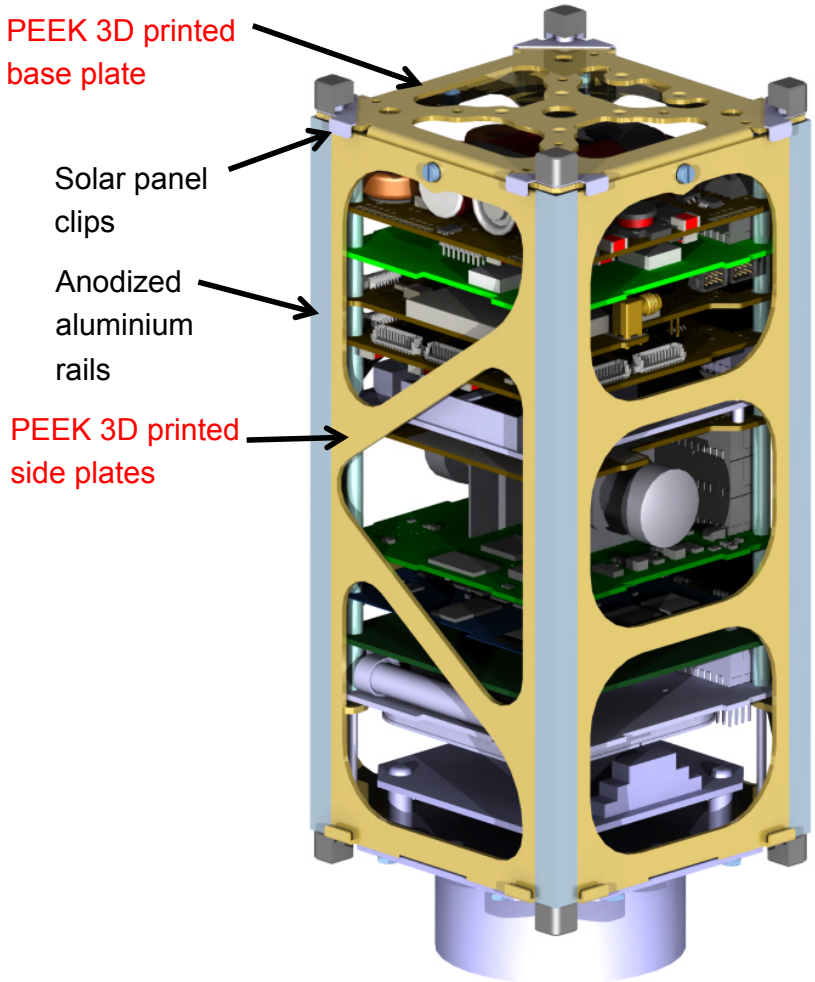
UNSW-EC0

A 2U CubSat comprising four UNSW/NICTA experimental payloads:

1. **Namuru: FPGA-based satellite navigation receiver**
   - Uses reflectometry to profile the ionosphere and troposphere, perform radio occultation experiments (atmospheric refraction of GPS signals), and to provide in-orbit position and velocity of UNSW-EC0
2. **RUSH: Rapid recovery from SEUs in reconfigurable hardware**
   - Evaluates FPGA-based SEU recovery approaches and maps the occurrence of SEUs for a non rad-hard Xilinx Artix-7 device in the thermosphere
3. **seL4 ROCS: Reliable Optimised Critical Systems**
   - Assesses the performance of critical systems utilising the seL4 microkernel
4. **RAMSES (RApid Manufactured SatellitE Structure)**
   - Evaluates use of 3D printing to provide CubeSat structure

UNSW-EC0





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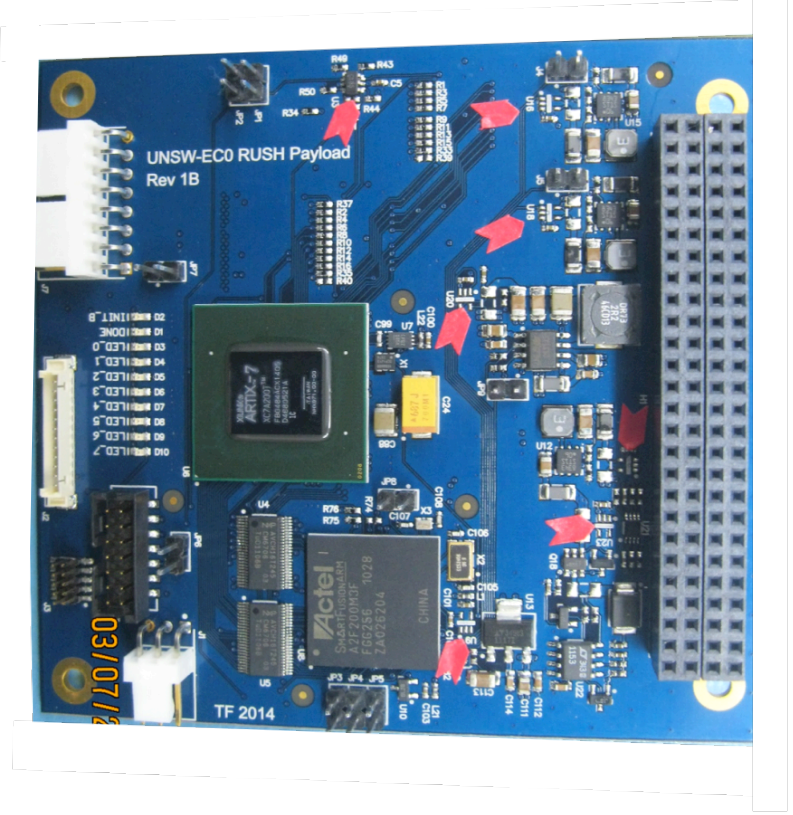
RUSH Payload Objectives

RUSH: Rapid recovery from SEUs in reconfigurable hardware

- **Evaluate new approaches to rapidly recover from SEUs in COTS FPGAs**
  - Evaluate the efficacy of a rapid PR-based SEU recovery approach on Xilinx Artix-7 XC7A200T FPGA
  - Benchmark results with respect to the traditional scrubbing approach
  - Obtain SEU occurrence rates, system recovery times, energy requirements and number of system resets to steer future research & development
- **Map SEU events in the thermosphere**
  - Provide a better understanding of the radiation performance of COTS 28nm Xilinx FPGAs in Low-Earth Orbit
- **Demonstrate in-orbit reconfiguration**



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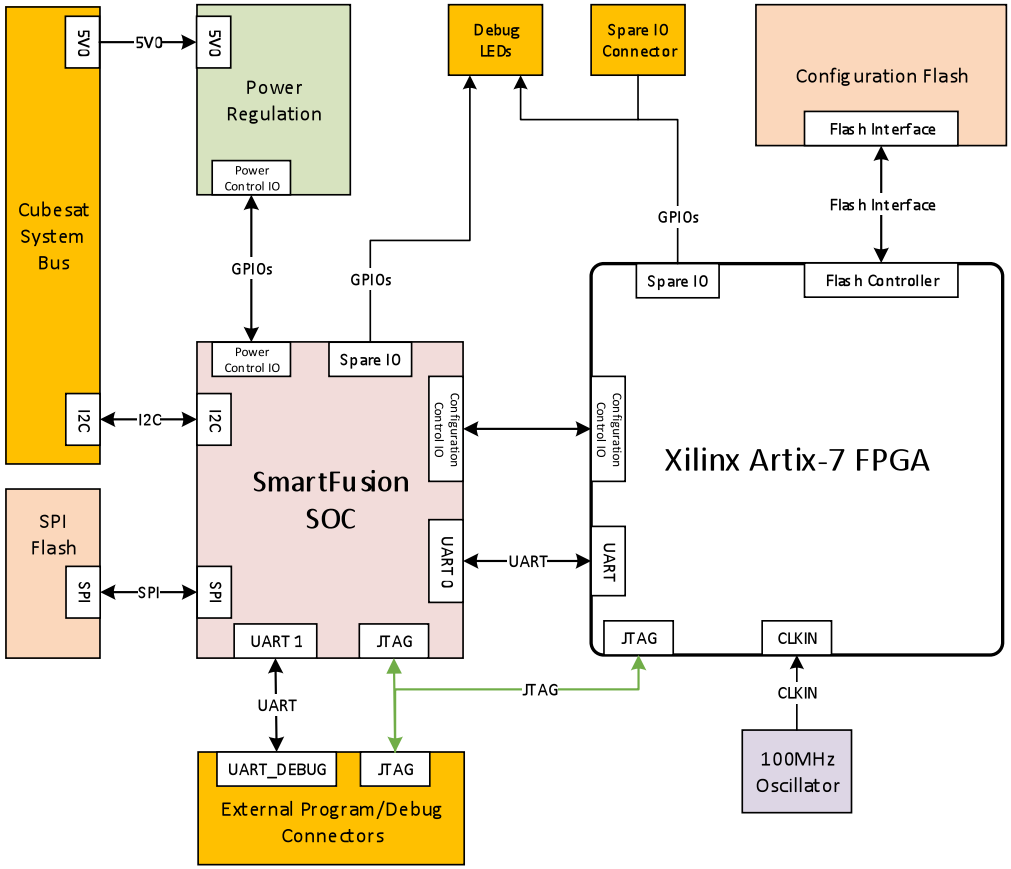
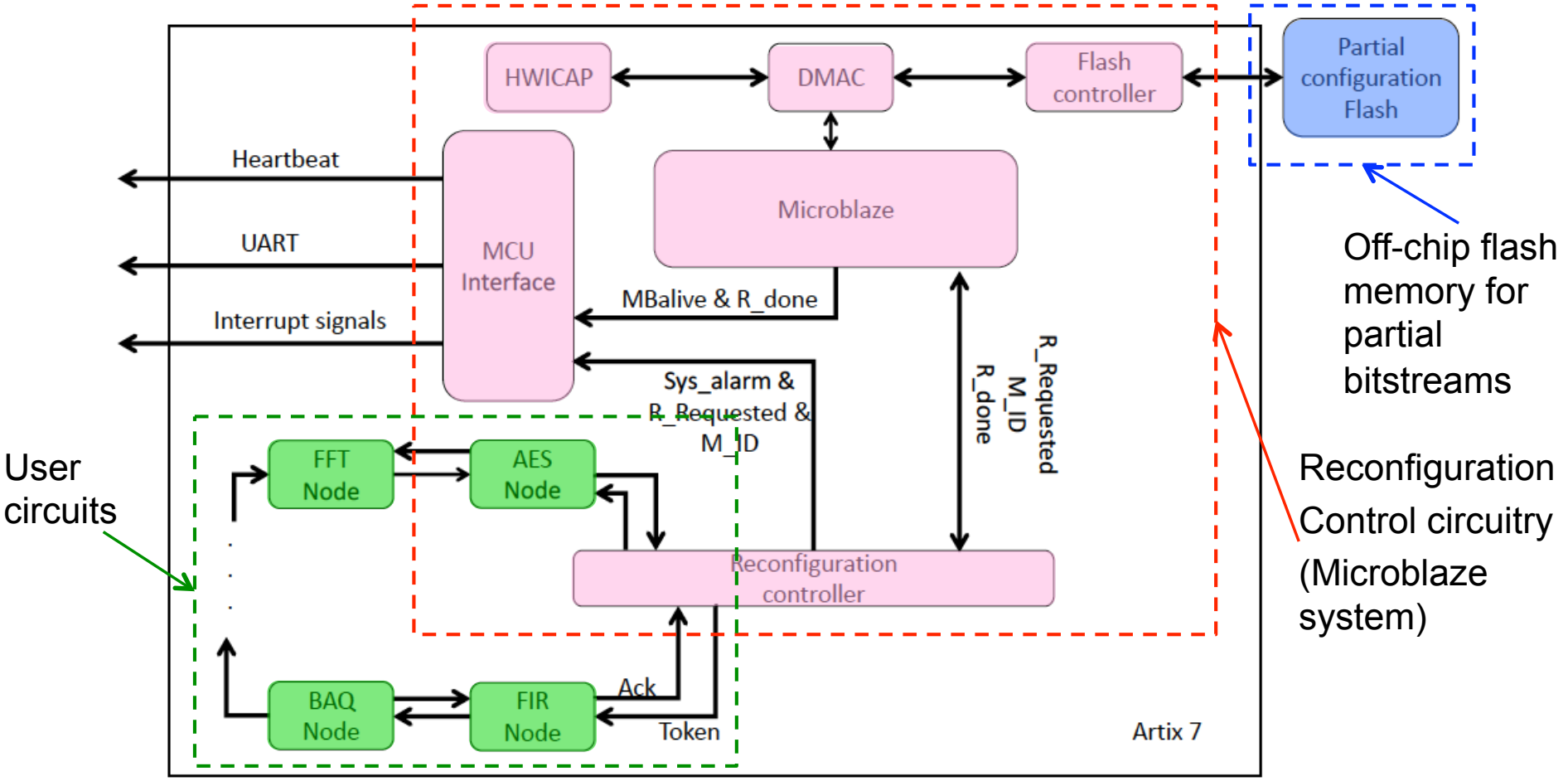
RUSH Configurations

Two base configurations:

- Scrubbing using SEM controller vs modular reconfiguration
- Similar TMR-based user circuits to enable comparison
- Circuits are representative of satellite tasks
  - JPEG, FFT, SAR, BAQ circuit components
- Assess SEU susceptibility
  - circuit area
  - resource type



Dynamic Modular Reconfiguration design



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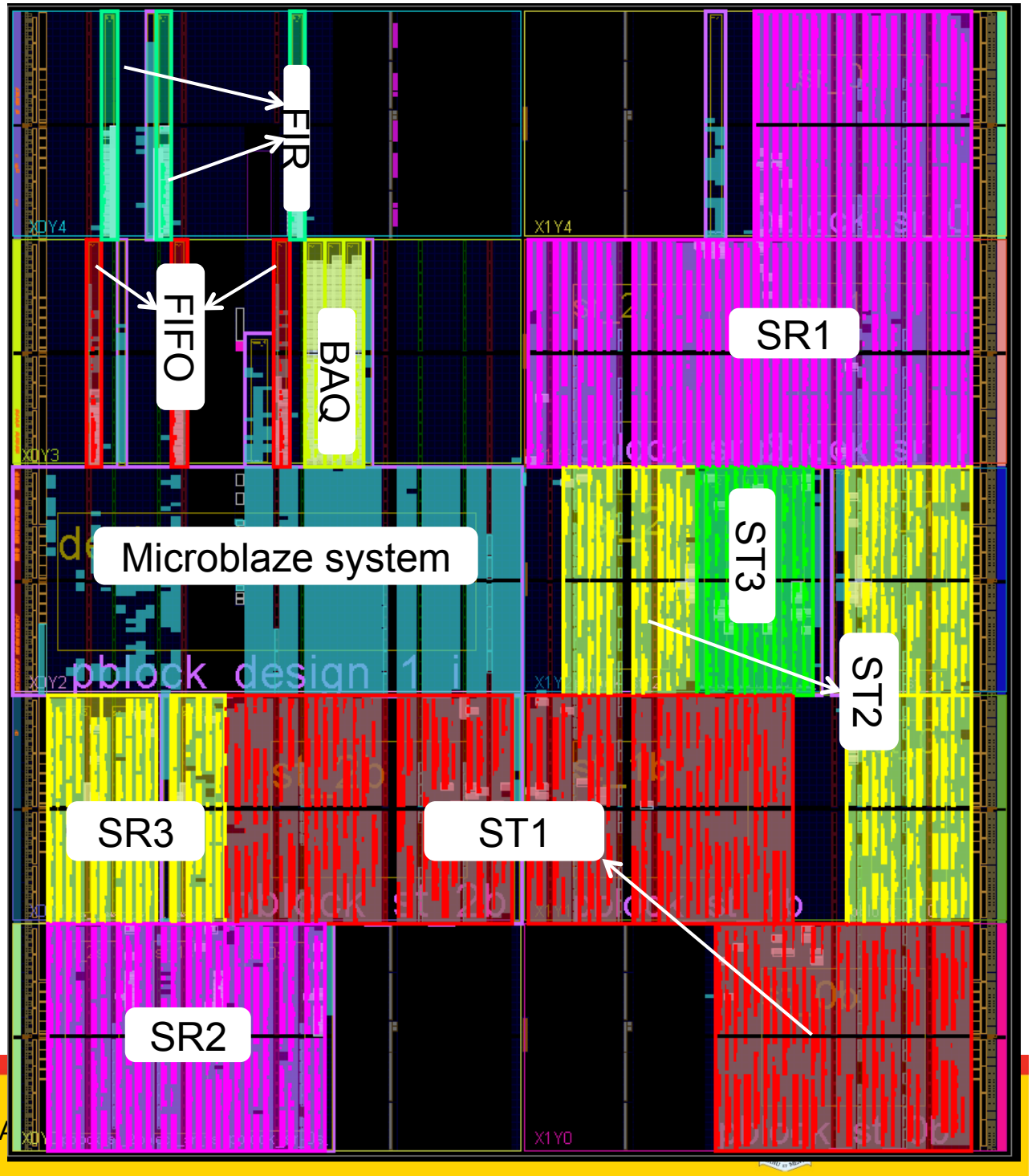
DMR floorplan

SR1	115x16-bit	40xDSP
SR2	80x16-bit	20xDSP
SR3	50x32-bit	Add only
ST1	32-leaf x 64-bit tree	31xDSP
ST2	32-leaf x 32-bit tree	31xDSP
ST3	16-leaf x 20-bit tree	Add only
FIFO	512x16-bit	
FIR	21-tap x 16-bit	32-bit MAC
BAQ	256x8-bit in; 3-bit out	

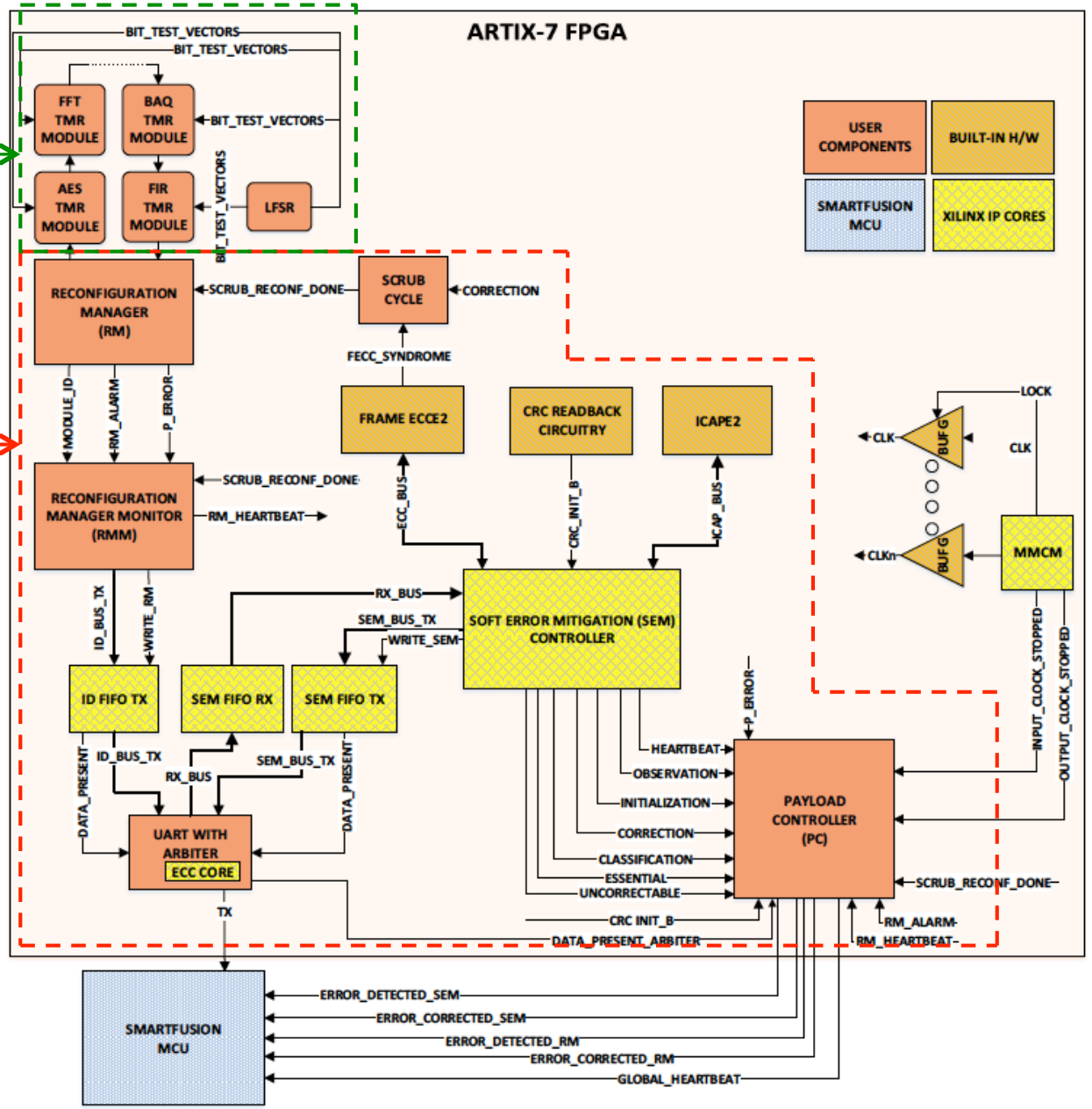


Scrubbing-based configuration

User circuits

Scrub controller and error log system

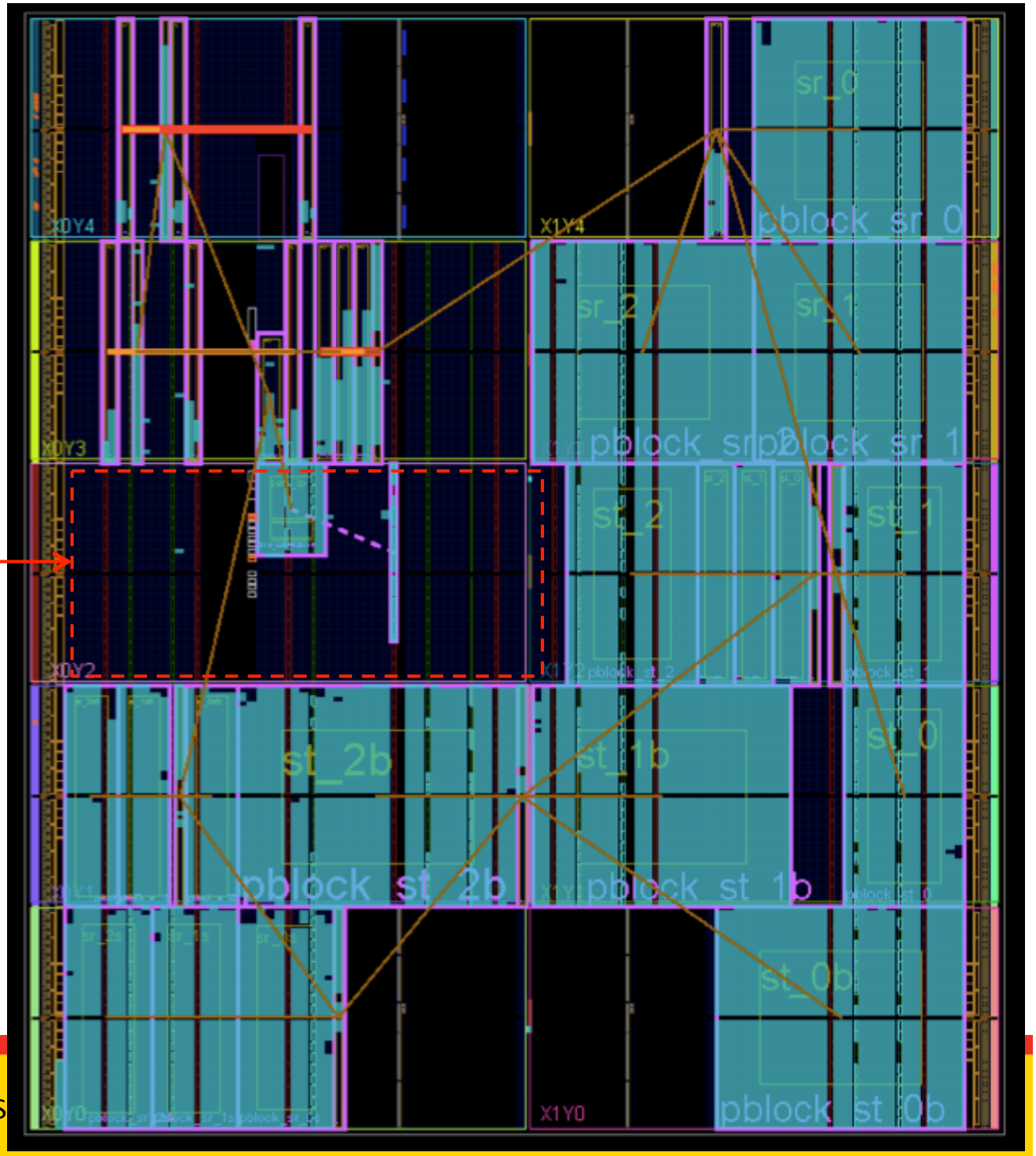
(replaces Microblaze system in DMR design)



Scrubbing floorplan

Scrub controller and error log system

(replaces Microblaze system in DMR design)



Work in progress

- Using configuration readback to check voters for error occurrence
- Combining scrubbing & dynamic modular reconfiguration for selective TMR
- Adapting the scrub frequency to the error rate
- Reliable heterogeneous design of a reconfiguration controller for space
- Design space exploration for FPGA-based heterogeneous systems meeting performance targets and reliability guarantees

Related work

- Carmichael et al, Xilinx scrubbing XAPP216, 2000
  - Also covers TMR techniques for FPGAs
- Selective TMR with scrubbing, for example
  - Samudrala et al, 2004+
  - Wirthlin et al, 2006+
- Several modular reconfiguration papers since 2004, for example
  - Kastensmidt et al, 2004+
  - Bolchini et al, 2007+
- FPGAs in space experiments
  - Cibola Flight Experiment – Los Alamos National Labs & BYU, 2007+
  - Sandria National Labs & NASA

Cibola Flight Experiment

- 2007 – 2014:
  - 3 boards x 3 rad-hard XQVR1000 FPGAs (6 Mbit bitstream size)
  - Launched into low-earth orbit
  - Scrubbing externally implemented with rad-hard components
  - Recorded 2,816 SEUs & 11 MBUs, but only operational 46% of the time
  - Equates to ~2 SEUs per operational day
  - 2007 – 2009 not operated over the South Atlantic Anomaly (SAA)
- 2011 launched Mission Response Module:
  - 2x rad-hard XQR4VLX200 (51 Mbit bitstream size) &
    2x rad-hard XQR4VSX55 (23 Mbit bitstream size)
  - Up 99.9% 10/2011 – 12/2012; operated 37% - 42% in the SAA
  - Recorded 11,330 SEUs, 6.37% MBUs & 5 Single Event Functional Interrupts
  - Equates to ~1 SEU per operational hour

What does the future hold?

COTS FPGAs

Built-in
SEM support

CMOS configuration
latch development

Architectural
experimentation

Thanks…

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Zhuoran Zhao

- Australian Centre for Space Engineering Research
- School of Computer Science and Engineering
- School of Electrical Engineering and Telecommunications
- Xilinx Inc.

- ICEMI Organizers