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Guest Editorial: Field-Programmable Technology

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Field-Programmable Technology (FPT) describes those electronic systems where the hardware as well as the software can be programmed on an application by application basis. Field Programmable Gate Arrays (FPGAs) represent the most common form of FPT, widely used in applications such as signal and image processing, telecommunications and computer networking. FPT continues to intrigue researchers; current research ranges from transistor-level programmable logic, through to high performance applications, and encompasses the design methodologies and design tools needed for such systems.

In "Reconfigurable Blocks Based on Balanced Ternary," Paul Beckett and Tayab Memon describe a new programmable logic block which takes advantage of some of the unique characteristics of Silicon-on-Insulator in order to deliver balanced ternary (−1,0,+1) logic functions and memory cells.

In "Using Data Contention in Dual-ported Memories for Security Applications", Tim Güneysu investigates the problem of how to protect design IP in a technology where hardware programs are difficult to secure. His paper explores device-specific behaviour during write collisions in dual-port FPGA memories to support IP protection.

For embedded systems that use floating point arithmetic, the choice has been fast hardware or slow software implementations. In "Improving Floating-Point Performance in Less Area: Fractured Floating Point Units (FFPUs)," Neil Hockert and Katherine Compton look at partial hardware support for floating point, which gives better performance than software floating point, and lower area than a full hardware unit.

As logic circuits get larger, the time for physical design at logic level discourages broad exploration of high-level architectural design alternatives. In "Rapid Synthesis and Simulation of Computational Ciruits in an MPPA," David Grant, Graeme Smecher, Guy Lemieux and Rosemary Francis present a tool flow (RVETool) for rapidly compiling computational circuits into a Massively Parallel Processor Array.

In "Automated Mapping of the MapReduce Pattern onto Parallel Computing Platforms," Qiang Lie, Tim Todman, Wayne Luk and George Constantinides explore using FPGAs effectively for large computational problems. Having identified that many applications use a "MapReduce" computational pattern, they develop a

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methodology to map such problems onto FPGA programmable hardware.

Also in the area of computationally intensive applications is "Implementation of the Longstaff and Schwartz American Option Pricing Model on FPGA," by Xiang Tian and Khaled Benkrid. Their paper shows that FPGAs are considerably more computationally efficient in both time and energy than conventional CPUs for the computing problem of financial product pricing.

These six papers will appeal to both the specialists in their individual areas, and also to those who wish a snapshot of the current breadth of FPT research.

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