# A Digital Ultra-Wideband Multiband Transceiver Architecture with Fast Frequency Hopping Capabilities

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## Abstract

This paper presents for the first time the circuit parameter analysis of a digital Multiband-UWB transceiver, encompassing a novel low-power sub-band generator. This sub-band generator is capable of producing multiple frequency bands, enabling sub-band generation from 3 to 10GHz with nanosecond switching times. The circuit analysis of the complete transceiver is used to set parameters of components. The analysis indicate that a LNA gain of 20dB, baseband amplifier gain of 45dB, matched filter accuracy of five bits, ADC accuracy of two bits, a 60dB dynamic range of the multi frequency generator, and frontend offset voltage of less than 30mV is required to achieve a 10dB SNR. Hspice simulation utilizing $0.35\mu m$ CMOS technology suggest that the power consumption of the sub-band generator is 8mW from a 1.8V power supply.

## 1. INTRODUCTION

Ultra-wideband (UWB) technology is being touted as the future of high-speed indoor wireless personal area networks. By communicating via short nanosecond pulses, UWB systems promise low power, high data rate communication while providing fine multipath resolution in the time domain [1]. However, the wide bandwidth, analogous to fine multipath resolution, requires UWB systems to operate in environments where interference from existing narrowband devices is crippling. Such interference cannot be eliminated by simple notch filtering as it causes time dispersion and spectral power loss of the received UWB signal[2]. Other interference mitigation techniques requiring frequency domain processing [3, 4] are less than ideal as they necessitate increased power consumption.

In light of such problems, a hybrid Multi-Band UWB (MB-UWB) approach has been proposed in [5, 6, 7]. As opposed to the traditional UWB approach where a single bandwidth of approximately 2-3 GHz is used for all data transmission, MB-UWB divides the available spectrum into channels (approximately 500MHz each). Data is then encoded in different channels at staggered time to provide multi-user access. Seven channels are shown in Figure 1. Each channel occupies 500MHz, and is spread from 3-7.5 GHz. Bands from 4.5 to 5.5 GHz are unused to avoid the UNII band. The desirable properties of the MB-UWB system include scalability, adaptability, and better co-existence with existing narrowband systems by dynamically avoiding interference dominated bands [5]. Since MB-UWB channels occupy a narrower band than traditional UWB, the pulse width is now wider, which enables the creation of such pulses with reduced effort. This means that the total system bandwidth is no longer limited by the time resolution of the pulse generating circuitry thus allowing full utilization of FCC's allocated band from 3 to 10 GHz, resulting in higher data rates. These benefits come at the cost of a more complex RF frontend and the challenging task of designing low power frequency generators to enable nanosecond channel switching.

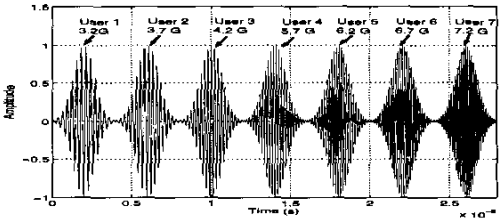


**Figure 1: Multiband Multiple-Access System**

If traditional UWB transceivers were to employ digital correlators, then the received signal has to be sampled at high Nyquist frequencies (for the 3-5GHz band, the sampling rate has to be at least 4GHz), which would consume excessive power. Thus, these UWB systems utilize analog correlators. MB-UWB signals occupy narrower bandwidth and therefore can utilize a lower speed ADC with digital correlators, improving scalability and flexibility.

The ability of MB-UWB systems to avoid interference affected bands is a major advantage over the traditional UWB systems. Traditional UWB systems with interference rejection capabilities can be found in [8, 9]. In [8], a low-power and low data rate system relying on notch filtering for interference mitigation was proposed. This system would suffer from high Q ringing effects described earlier. A minimum mean square error multiuser detection receiver introduced in [9] successfully rejects narrowband interference, but requires a high dynamic range and high speed ADC, making it impractical for portable systems where power performance is critical.

Despite the numerous published architectures dealing with MB-UWB architectures, none have reported the exploration of such systems using circuit parameter analysis. In this paper we describe a digital MB-UWB transceiver architecture, and characterize it using circuit parameters. The proposed architecture which contains a low power multi-frequency generator (MFG) for fast frequency hopping, is robust to narrowband interference, and requires no filtering or power intensive in-

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terference processing.

In Section 2, the proposed transceiver architecture is described. The fast MFG circuit is presented in Section 3. Circuit parameters and mathematical derivation of their impact on the signal to noise performance of the system is analyzed in Section 4, followed by conclusions in Section 5.

## 2. SYSTEM ARCHITECTURE

The proposed architecture, as shown in Figure 2, consists of an analog frontend and performs the correlation in the digital domain. The system operates in the 3-10GHz range, in 500 MHz channels. The channels in which narrowband interference is prominent are unused. The I and Q streams support both QPSK and BPSK modulation as proposed by [6, 7] for easier adaptation with different channel conditions and system bandwidth requirements. An MFG is used to switch between channels.

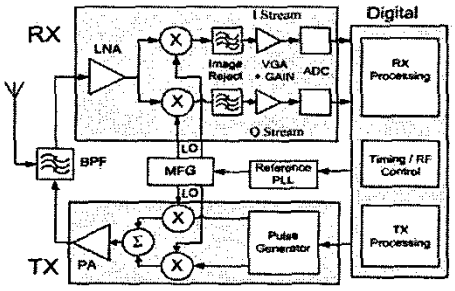


**Figure 2: System Diagram**

This system operates in a direct conversion mode whereby a baseband UWB signal generated by the pulse generator is placed in the desired frequency channel by an up-conversion mixer. This signal is then amplified and transmitted over a non-resonating wideband antenna. On the receiver side, signal from the antenna propagates through wideband gain stages and is down-mixed to the baseband where additional gain is provided, before being sampled by the ADC.

### 2.1 Antenna

Due to the short pulse UWB signal, the antenna must be wideband and non-resonating. In the 3 to 10 GHz range, omnidirectional antennas with low Q and high radiation efficiency are difficult to design. While Transverse Electro-Magnetic (TEM) horn antennas and log-periodic antennas exhibit frequency independence, their radiation patterns are directional[10]. An omnidirectional, low voltage standing wave ratio (VSWR) antenna designed for UWB applications has been reported in [10]. Other antennas such as the Large Current Radiator are also suitable for this system[11].

### 2.2 RF Frontend

The receive chain in Figure 2, integrates a 3-10GHz bandpass filter, a low noise amplifier (LNA), a set of active I/Q down-conversion mixers driven by a quadrature generator, a set of baseband amplifiers and variable gain amplifiers (VGA). The image reject filter between the LNA and the mixer is eliminated since a homodyne architecture is adopted. Differential circuit topology is employed throughout the analog frontend, to combat digital switching noise coupled through the substrate, and to minimize back-radiation of local oscillator (LO) signal through the antenna. The entire frontend is to be implemented in SiGe technology which can be integrated with CMOS digital logic in a single process, enabling an integrated, single chip solution.

The bandpass filter attenuates out of band noise and interference. This filter can have a low Q factor since the filter pass band is several gigahertz wide. This low Q factor will not cause ringing and the resulting time dispersion of the UWB signal.

The LNA is designed for moderate gain due to the difficulty in designing wideband, high gain amplifiers, and to avoid saturating the down-conversion mixer. The remaining system gain is contributed by the baseband amplifier operating from DC to 500MHz. In addition, the amplification stages are designed for fast overload recovery to prevent prolonged overloading of the frontend.

The LNA is followed by a set of down-conversion mixers driven by quadrature LO signals derived from the MFG. These quadrature signals are generated by RC delay branches, which must maintain I/Q phase differences to within five degrees from quadrature. The mixers are active as they have lower noise figure (NF) and provide insertion gain. A buffer stage is placed at the output of the quadrature generator to maintain sufficient LO drive, which optimizes mixer linearity and noise performance [12]. Subsequent stages include a set of low pass anti-aliasing filters and variable gain amplifiers (VGA) to condition the I/Q baseband signals and match the full scale input range of the ADCs. The VGA is controlled by an automatic gain control loop consisting of a detector, a low pass filter and a difference amplifier.

The transmit chain is relatively simple and consists of a pulse generator, quadrature modulator and a power amplifier. The quadrature modulator frequency up-converts the quadrature baseband inputs and sums the output current signals. The power amplifier then provides power gain to drive the antenna.

### 2.3 ADC and Digital Backend

The ADC is configured as a two bit flash converter (derived in Section 4) operating at 1GS/s. Time and frequency interleaving was not employed because a 2 bit flash converters are relatively low power and do not suffer from SNR degradation due to gain mismatch and sampling jitter [13]. The correlation receiver is based on a digital RAKE receiver utilizing parallel matched filters operating at one nanosecond time offsets. The correlation results are then recombined and decoded into binary data.

## 3. MULTI-FREQUENCY GENERATOR

An MB-UWB system requires rapid switching between channels at different frequencies. Traditional frequency hopping spread spectrum (FHSS) systems, such as Bluetooth, use a single programmable phase locked loop (PLL) for channel selection. This solution is feasible in Bluetooth systems, since the hopping period is only required to be in the order of hundreds of microseconds.

A programmable PLL is not viable for nanosecond switching speeds of MB-UWB, because the PLL's locking time is usually limited to $\frac{1}{10}$ of its loop bandwidth to ensure stability. A switched PLL bank is power intensive, since each PLL alone dissipates approximately 10mW. A low power, 3-7 GHz single PLL MFG, consuming 39mW has been proposed in [14]. In this section, a new low power design, with a novel sub-band generation method is presented.

The MFG, shown in Figure 3, integrates buffered VCO, a PLL, a sub-band generator (SBG), a passive mixer and RF switches. The buffer connecting the output of VCO to the PLL provides isolation and prevent LO pulling [12]. The PLL provides the fundamental frequency used by the SBG to generate multiple frquencies from DC to 3.12 GHz at 520 Mhz offsets. Each of the sub-frequencies are connected to a switch acting as a multiplexer, allowing controllable mixing with the fundamental frequency to produce the desired frequency output.

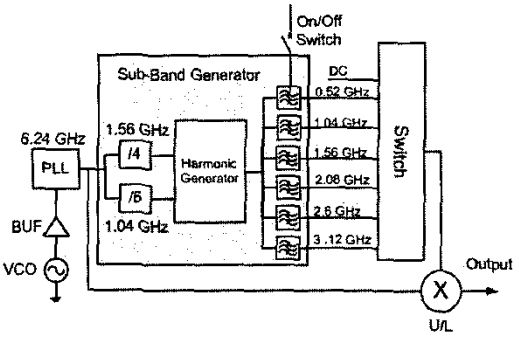


**Figure 3: Multi-Frequency Generator**

The sub-band generation exploits the strong non-linearity of harmonic generators such as single transistor mixers. Classical non-linear analysis describes the input-output relationship with a power series expansion:

$$V_{out} = \sum_{n=0}^{N} c_n (V_{in})^n$$

Setting the input signal to be the sum of two sinusoids:

$$V_{in} = V_{f_1} cos(\omega_{f_1} t) + V_{f_2} cos(\omega_{f_2} t),$$

will produce output

$$V_{out} = V_{fund} + V_{harmon} + V_{IM}$$

In cases where first and second order non-linearity dominates, the $V_{fund}$ term contains the original input frequencies $f_1$ and $f_2$. $V_{harmon}$ term contains DC offset as well as second harmonics of the input signals $2f_1$ and $2f_2$. The final component $V_{IM}$ contains the intermodulation products with the frequencies $f_1 - f_2$ and $f_1 + f_2$. The fundamental and harmonic terms are generally undesirable for the normal application of up and down-conversion. However, they are suitable for generating multiple frequencies that are easily controlled. Even though 520MHz sub-band separation was demonstrated by the example in Figure 3, desired frequencies can be obtained by setting the input frequencies $f1$ and $f2$ to twice and three times the sub-band separation. In addition, 3rd and 4th order non-linearities can also be exploited to generate upper frequencies, which cannot be generated by the MFG in [14]. The harmonic frequencies, however, have different amplitudes and must be compensated by subsequent stages to ensure constant amplitude modulation.

The harmonic generator connects to a bank of switched band pass filters (BPF). These high Q, 6th-order fully differential BPFs are based on the gyrator-C inductor topology and consumes only 6.8mW [15]. Power consumption is minimized since only a single BPF need to be operational at any given time. Hence, the BPFs must be designed for fast on and off time to maintain fast switching speed while saving

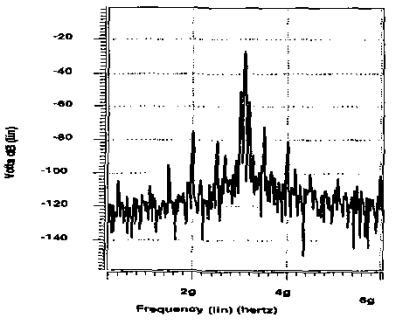


**Figure 4: Sub-band Generator Output**

power. Passband gain of these BPFs can also be individually tuned to compensate for amplitude mismatches in different sub-bands.

The harmonic generator and BPF combination was simulated in Hspice using a 0.35 $\mu m$ CMOS process. Figure 4 shows a sample 3.1 GHz sinusoidal output. The adjacent sub-bands are approximately 50 dB weaker than the main signal. The noise floor is approximately -90dBc/Hz, which equates to -75dBc/Hz at the output of the MFG assuming a 15dB NF for the mixer and switch. The power consumption of the simulated circuit was 8.2mW, which appears at least comparable with the 18mW MFG in [14].

Simulation to date indicate adjacent channel isolation to be comparable with the MFG in [14], which offers 23 dB adjacent channel rejection. Such a comparison is valid since the only difference is the methods of generating the sub-bands.

## 4. SYSTEM PARAMETER DERIVATION

In this section, the effect of varying system offset, gain, ADC and matched filter accuracy, and the dynamic range of the MFG, on the system's signal to noise ratio (SNR) is formulated. The results of these formulations are used to compare different circuit configurations.

A typical UWB received signal after ADC can be expressed as:

$$R = S + N + P + O + Q_r$$

where each of the variables $S$, $N$, $P$, $O$, $Q_r$ *and* $R$ are vectors of length $\frac{w}{f}$., where $w$ is the capture window length and $f$ is the sampling frequency of the ADC. Hence, $S = [s[0]\ s[1] \cdots s[\frac{w}{f} - 1]]$ and represents $\frac{w}{f}$ samples of the desired UWB pulse. N is the captured thermal noise introduced by the channel. This noise is zero mean with variance contributed to by the temperature, frontend NF, power gain and the baseband filter bandwidth. $P$ represents Gaussian noise induced by other UWB devices through reciprocal mixing and has variance equal to the product of wideband noise floor, and the signal strength of nearby interferers. $O$ is the offset voltage at the input of the ADC. It is an additional noise source in the receiver chain and will determine the minimum system gain necessary to ensure accurate sampling. $O$ is assumed to be Gaussian with variance of ${V_{off}}^2$. $Q_r$ is the quantization error of the ADC due to the finite accuracy of digitization. Assuming an ideal converter, $Q_r$ is zero mean with variance of $\frac{V_{lsb}^2}{12}$.

The matched filter coefficients are represented digitally and

the impact of analog non-idealities are minimal. The template signal can be defined as:

$$T = S + Q_m$$

where S is the desired UWB pulse and $Q_m$ is the quantization error of the matched filter coefficients. The quantization error is Gaussian distributed with a variance of $\frac{V_{lsb}^2}{12}$.

The matched filter is based on a FIR filter structure. Each sample of the received signal is multiplied with the template and then summed to obtain the correlation coefficient which is then decoded. Hence, the output of the matched filter is:

$$M = TR^T$$

SNR is defined as:

$$\frac{E(M)^2}{E(M - E(M))^2}$$

and $E(M) = SS^T = S^2$, since all the noise terms are Gaussian and have an expected value of zero. The expanded term for $E(M - E(M))^2$ can be simplified since each of the noise terms are independent Gaussian variables.

Variance of a Gaussian distributed variable $x$ is:

$$E(x - E(x))^2 = E(x^2) - E(x)^2 = E(x^2)$$

Hence the overall SNR is shown to be:

$$\frac{S^4}{S^2(\sigma_N^2 + \sigma_P^2 + \sigma_{Qr}^2 + \sigma_O^2 + \sigma_{Qm}^2) + \sigma_{Qm}^2(\sigma_N^2 + \sigma_P^2 + \sigma_{Qr}^2 + \sigma_O^2)}$$

This equation is used to study the effect of varying each of the circuit parameters suche as gain noise etc. [16] has shown that with a six arm RAKE receiver, a Bit Error Rate (BER) of $10^{-3}$ is achieved under severe multipath fading conditions with a corresponding SNR of 10dB. Therefore, a 10dB SNR is used as a benchmark in subsequent discussions.

## 4.1 ADC and Matched Filter Accuracy

The system SNR is plotted against the number of ADC bits for various matched filter bit widths and shown in Figure 5. The system parameters used for the derivation are summarized in Table 1:

| Parameter | Value |
|---|---|
| UWB signal energy | -74dBm at 50Ω |
| Signal bandwidth | 500Mhz |
| LNA gain / NF | 20dB/4dB |
| Baseband gain / NF | 45dB/15dB |
| Offset voltage | 10mV |
| MFG noise floor | -60dBc/Hz |
| MUI condition | 9 interferer, -20dB SIR |
| Coding gain | 6dB |

**Table 1: System parameters for ADC bitwidth analysis**

Figure 5 shows that for all matched filter bit widths, the SNR increases by almost 1dB when the number of ADC bits is increased from one to two. This SNR improvement slowly plateaus and become insignificant when the ADC bit width is larger than three. Since the power of flash ADCs increase exponentially with accuracy, a two bit ADC is chosen as a compromise between improving the SNR and adding excessive power consumption.

In terms of matched filter bit widths, the improvement in SNR becomes inconsequential as filter accuracy is increased. To maximise the SNR, the five bit matched filter was chosen. The energy consumption of increased matched filter accuracy is not a concern as the digital multipliers are low powered when compared to the ADC.

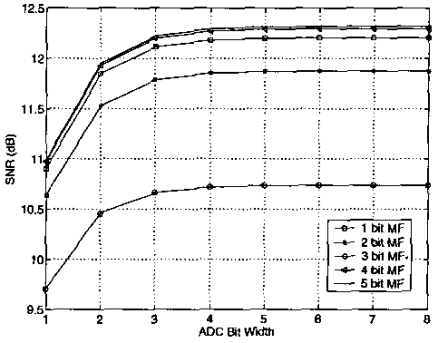


**Figure 5: SNR vs ADC bit**

## 4.2 Gain and Offset Voltage

The system gain and offset voltages are closely related. This is due to the requirement for the UWB signal to have sufficient amplitude to overcome the inherent offset error, and to trigger the input comparator of the flash ADC accurately.

Figure 6 shows the SNR achieved with different gain and offset combinations. The results show the prominent effect of offset on SNR at low system gain. As expected, this negative effect is decreased when system gain is increased, indicated by the slower roll off in SNR at greater offset voltages. However, a total gain of 65 dB was chosen as circuit with gain of 70dB or greater is difficult to achieve. This implies that a low offset voltage of below 30mV is required to maintain the 10dB SNR target. Therefore, without capacitive coupling between stages or other offset cancellation techniques, offset remains a dominant source of error even at moderately high gains.

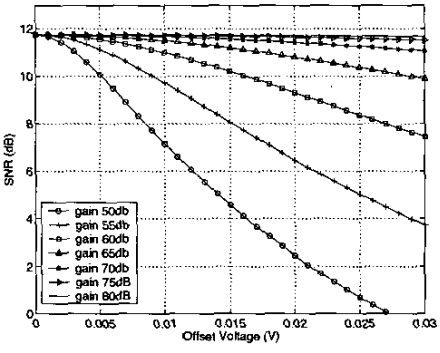


**Figure 6: SNR vs Offset Voltage**

## 4.3 Gain Distribution

Intuitively, increasing the LNA gain contribution reduces the system NF and improves the SNR. LNA gain, however, must be limited to avoid saturating the subsequent stages. With the total system gain fixed at 65dB, combinations of the LNA and baseband gain are investigated to determine the minimum required LNA gain.

Figure 7 indicates approximately 1dB SNR penalty when the LNA gain is decreased to 15dB from 20dB. On the other

hand, only 0.5dB SNR improvement is achieved by increasing LNA gain to 25dB. Thus, 20dB LNA gain is chosen as the nominal value.

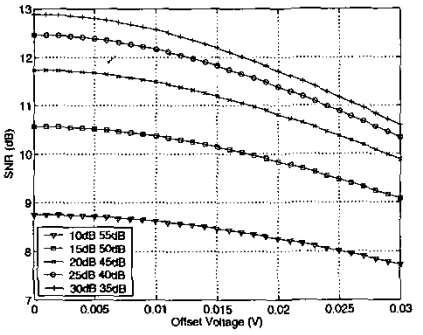


**Figure 7: SNR for Various Gain Distribution**

## 4.4 MFG Dynamic Range

Wideband noise of the MFG can induce strong adjacent channel noise from other close-in UWB devices due to reciprocal mixing and the near-far effect. Therefore, increased wideband noise will elevate the baseband noise floor and reduce the sensitivity of the receiver. In addition, noise close to the carrier frequency directly contributes to the in-band noise. These effects places a lower bound on the dynamic range of the MFG.

Figure 8 shows the effect of nine simultaneously transmitting interferers at various interference to signal ratios when the intended user is 10 meters away from the receiver. For low levels of interference where the near-far effect is not prominent, the lowering of the MFG's noise floor is not necessary. As the interference level increases to 8dB, which corresponds to interferers being four meters away from the receiver, dynamic range requirements are still easily met, since the the SNR penalty in going from -90dBc/Hz to -50dBc/Hz is less than 0.5 dB. At the extreme case where the interference to signal ratio is 20dB (interferers at one meter away), a dynamic range of 60dB is required to bound the SNR penalty to within 0.5dB. Since the MFG design presented had a 75dB dynamic range, it is within the level required.

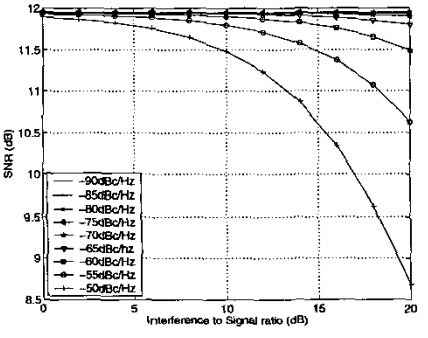


**Figure 8: SNR vs Multi-user Noise**

# 5. CONCLUSIONS

An architecture of a digital MB-UWB transceiver suitable for high rate personal area network applications has been presented. The transceiver contains a novel single PLL, low power multi-frequency generator to allow fast channel switching. Circuit issues including gain distribution, offset , ADC accuracy, noise figure and dynamic range were examined in relation to their impact on system performance. The analysis has shown that a 20dB LNA gain, 45 dB baseband amplifier gain, five bits matched filter, two bits ADC, a 60dB multi frequency generator dynamic range, and frontend offset voltage of less than 30mV is required to achieve a 10dB SNR.

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