ADC Precision Requirement for Digital Ultra-Wideband Receivers with Sublinear Front-ends: a Power and Performance Perspective

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Abstract

This paper presents the power and performance analysis of a digital, direct sequence ultra-wideband (DS-UWB) receiver operating in the 3 to 4 GHz band. The signal to noise and distortion ratio (SNDR) and bit error rate (BER) were evaluated with varying degrees of front-end linearity and analog to digital converter (ADC) accuracy. The analysis and simulation results indicate two or more ADC bits are required for reliable data reception in the presence of strong interference and intermodulation distortion. In addition to BER performance, power consumption of different hardware configurations is also evaluated to form the cost function for evaluating design choices. The combined power and performance analysis indicates that starting with one-bit ADC resolutions, a substantial gain in reliability can be attained by increasing ADC resolution to two-bits or more. When the ADC resolution improves beyond three bits , front-end linearization achieves similar BER improvements to increasing the ADC accuracy, at a fraction of the power cost. As a result, linear front-end designs become significant only when high precision ADCs are utilized.

1. Introduction

The UWB radio is a new technology that continues to generate considerable interest for its usage in both military and consumer communication applications. Recently, several standards based on pulse and orthogonal frequency division multiplexing (OFDM) have been proposed to realize UWB wireless personal area networks. By communicating via short nanosecond pulses, pulse based UWB systems promise low power, high data rate communication while providing fine multipath resolution in the time domain, unmatched by existing narrowband systems [1]. Currently, commercial UWB applications have been approved by the Federal Communications Commission to operate in the 3 to 10 GHz band under a power emission limit of -41.3 dBm/MHz. Although its operating distance is restricted, power limited UWB signals can lead to low power, high performance implementation of the front-end circuitry.

For traditional high power, narrowband radio systems, non-linearity in the receiver front-end generates undesirable distortion, leading to in-band and adjacent channel interference. As a result, reliable performance can be obtained only through the use of highly linear analog front-ends [2]. For pulse based UWB systems, the received signal is broadband with low peak to average power ratio. Therefore, stringent front-end linearity requirement of narrowband receivers may no longer be necessary. The authors in [3] have demonstrated that pulse doublets can be used to mitigate non-linearity induced distortion. Thus, radio frequency (RF) circuits can be greatly optimized for other performance metrics such as noise, power and gain by trading off linearity. Area savings derived from reduced linearization circuitry also drive down production cost and offer greater commercialization advantages. However, the analysis presented in [3] was only applicable to analog correlation based receivers since the impact of ADC quantization on pulse doublets was not evaluated.

Digital UWB receiver architectures have been proposed by [4, 5] as digital correlation offers considerable flexibility and technology scaling benefits. An example of a digital receiver is shown in Fig. 1. The ADC is a key block in the digital receiver chain, having a large impact on overall power dissipation and system performance. Due to the wide bandwidth of the UWB pulse, the lower bound imposed by the Nyquist theorem on the sampling rate is typically in the GHz range. Efficient implementations of such high speed ADCs mandate the use of flash architectures which exhibit an exponential increase in comparator area and power with the resolution specification. State of the art flash ADCs reported in [6], [7], and [8] have a maximum resolution of six bits while consuming significant power and occupying substantial chip area.

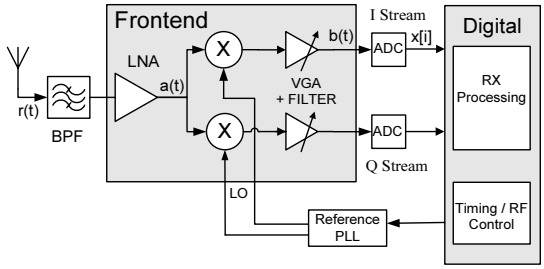

Figure 1: Digital UWB receiver system diagram

Steep tradeoffs between the ADC's performance and implementation costs have prompted authors in [4, 5] to investigate the minimum precision necessary to maintain accurate data detection. Authors in [4] have shown that four bits are sufficient for reliable detections of UWB signals under both additive white gaussian noise (AWGN) and narrowband interference (NBI) dominated cases. In contrast, authors in [5] proposed that only a single bit is required under severe NBI. Their analysis concentrate mainly on system reliability without evaluation of power usage. In addition, the effect of ADC precision on digital UWB systems working with sublinear front-ends and possible trade-offs with linearity are yet to be addressed.

This paper presents, for the first time, digital UWB system's SNDR and BER performance considering interference power and frequency, ADC precision, and RF circuit non-linearity characteristics. When combined with detailed power analysis, we demonstrate that at least two quantization bits are necessary to maintain accurate detection. Furthermore, our investigation indicates that careful trade-off between front-end linearity and ADC accuracy is required when designing UWB receivers with power and performance.

This paper is organized as follows. In section 2, we describe the receiver linearity model using Taylor-series analysis, followed by an introduction to the UWB receiver system model. Mathematical equations are formulated in section 3 to investigate SNDR and BER performance in the presence of NBI, under varying circuit nonlineariy and ADC precision. Section 4 estimates power usage for the ADC and common front-end components such as low noise amplifiers(LNA), mixers and baseband amplifiers. The theoretical formulas presented in Sections 3 and 4 are employed in Section 5 to analyze the tradeoffs between power consumption, linearity and ADC precision. Pareto optimal configurations in the full design space are then

Proceedings of the 19th International Conference on VLSI Design (VLSID'06)
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evaluated and discussed. Conclusions are drawn in Section 6.

2. System Model

2.1 Non-linearity Model

RF circuits commonly behave in a weakly non-linear fashion under normal operating conditions and have been analyzed using different techniques in the literature [9, 10]. In this paper, we employ a non-linear memory-less model for analog circuits with no frequency dependency, which can be characterized as follows:

$$Y(t) = \alpha_0 + \alpha_1 x(t) + \alpha_2 x(t)^2 + \alpha_3 x(t)^3 + ... \quad (1)$$

where x(t) is the input to the system and α_ns are the n^{th} order coefficients of non-linearity. The effect of non-linearity can be observed by setting the input to two signals with amplitudes V_{f_1} and V_{f_2}, and frequencies $\frac{\omega_{f_1}}{2\pi}$ and $\frac{\omega_{f_2}}{2\pi}$ respectively:

$$V_{in} = V_{f_1} cos(\omega_{f_1} t) + V_{f_2} cos(\omega_{f_2} t),$$

The output

$$V_{out} = V_{fund} + V_{harmon} + V_{IM}$$

will contain undesired harmonic and intermodulation components not present in the input. Due to the wide bandwidth occupied by UWB signals, these component often appear in the operating band and corrupt the signal of interest. The strength of the intermodulation products can be measured by the input third order intermodulation intercept point:

$$IIP_3 = \sqrt{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|} \quad (2)$$

which is defined as the input amplitude at which the third order intermodulation tones are equal to the fundamental tone. Non-linearity also causes small signal gain compression and reduces the signal gain with increasing input level.

2.2 DS-UWB System Model

In a direct sequency ultra-wideband (DS-UWB) system with N_p piconets each with N_u users, multiple access within each piconet is achieved via a time division multiple access (TDMA) scheme, while co-locating piconets communicate using code sequences with low cross-correlation. In the p^{th} piconet, user k's DS-UWB transmitted pulse train using bi-phase modulation is

$$u_k^p(t) = \sum_{j=1}^{N_c} f_j^p \beta_k w(t - jT_f - c_j^k T_c) \quad (3)$$

where N_c is the total number of pulses in the pulse train, j is the pulse number, T_f is the frame time, T_c is the chip duration and c_j^k is the k^{th} user's random hopping sequence. The transmitted Gaussian monopulse is bi-phase modulated by binary data sequence β_k and piconet code sequence f_j^p for p^{th} piconet to form the transmitted signal. This signal is processed by the receiver shown in Fig. 1

The received signal at the output of the antenna-filter submodule can be characterized as:

$$r_k(t) = \left(A_k u_k^p(t - \tau_k) + I(t) + n(t)\right) \circledast h_{RF}(t) \quad (4)$$

where $A_k u_k^p(t-\tau_k)$ is user k's received UWB signal with amplitude A_k after delay of τ_k and

$$I(t) = \sum_{n=1}^{N} V_n(t) cos(\omega_{f_n} t + \phi_n(t))$$

represents the narrowband interferences with amplitude $V_n(t)$, frequency $\frac{\omega_{f_n}}{2\Pi}$ and random phase $\phi_n(t)$, while n(t) is the white channel noise with variance contributed by the temperature and the filter bandwidth. Symbol $\circledast$ denotes the convolution operation and $h_{RF}(t)$ is the impulse response of the pre-select filter.

The received signal $r_k(t)$ is then amplified by the non-linear wideband LNA. Due to $r_k(t)$ being a combination of periodic and stochastic signals, precise mathematical representation of the signal at the output of the non-linear system is non-trivial. However, it is not difficult to see that the output will consist of a linear replica of the input signal and an error signal. The linear replica contains only the desired fundamental terms. The error signal is introduced by the non-linear response, producing strong narrowband spectral components and distortion from the stochastic signals. Without loss of generality, only the *I* channel of the receiver is examined. After down conversion and baseband gain and filtering stages, a baseband signal $b_k(t)$ is produced:

$$b_k(t) = \left[a_k(t) V_{f_c} cos(\omega_{f_c} t + \phi(t))\right] \circledast h_{LP}(t) \quad (5)$$

where $a_k(t)$ is the signal from the output of the LNA, and f_c is the centre frequency of the desired UWB signal. This baseband signal $b_k(t)$ is then sampled and quantized by the ADC, producing signal $X[i]$ which is digitally correlated with the template signal to compute the decision statistic d. Each of the LNA, down-conversion mixer and baseband gain stages are modeled by a Taylor series with non-linear coefficients set by overall receiver IIP_3 and gain requirements. The next section will formulate the relationship between distortion and ADC precision in order to examine their impact on system SNDR and BER.

3. ADC Performance Analysis

After the digitization process, signal at the output of the ADC can be expressed as:

$$X[i] = S[i] + I[i] + N[i] + Q[i] \quad (6)$$

where each of the variables X, S, I, N and Q are vectors of length $\frac{l}{T_s}$, where $l = N_c T_f$ is the capture window length and T_s is the sampling interval of the ADC. Hence, $S = [s[1]\ s[2] \cdots s[N_c \frac{T_f}{T_s}]]$ and represents samples of the desired UWB pulse. I represents the narrowband interference and distortion effects due to front-end non-linearity. N is the Gaussian thermal noise introduced by the channel with variance set by the temperature, noise figure, power gain and the bandwidth of the front-end circuitry. The last term Q represents the quantization error of the ADC due to the finite accuracy of digitization. Assuming an ideal automatic gain control circuitry and ADC, Q is gaussian with variance of $\frac{V_{lsb}^2}{12}$, where $V_{lsb} = \frac{|X-Q|}{2^b-1}$ is the quantization step size.

After correlation against a template signal $T[i]$, the digital correlator produces decision statistic d_m for user k's m^{th} received symbol. Without loss of generality, perfect synchronization between the template and the received signal is assumed and the decision statistic of the first symbol is expressed as :

$$d_1 = \sum_{i=1}^{\frac{l}{T_s}} X[i] \cdot T[i] = s_1 + I_1' + n_1' + m_1' + q_1' \quad (7)$$

where

$$s_1 = \sum_{i=1}^{\frac{l}{T_s}} \beta_1^k (\alpha_1 - \chi) A_k f_j^p w[i] \cdot A_k f_j^p w[i] \quad (8)$$

corresponds to the signal portion at the output of the correlator and evaluates to

$$s_1 = N_c (\alpha_1 - \chi) A_k^2 \beta_1^k R_{ww} \quad (9)$$

where $R_{ww} = \sum_{i=1}^{\frac{l}{T_s}} w[i] \cdot w[i]$ is the autocorrelation function of the received waveform and

$$\chi = \frac{3}{4}\alpha_3 A_k^3 + \frac{3}{2}\alpha_3 A_k \sum_{n=1}^{N} V_n^2 \quad (10)$$

is the signal compression factor and is a function of the 3^{rd} order non-linearity coefficient α_3, number of narrowband interferers, and their maximum signal strength. The term

$$I_1' = \sum_{i=1}^{\frac{l}{T_s}} \xi[i - jT_f - c_j^k T_c] \cdot f_j^p w[i] \tag{11}$$

accounts for the effect of external interferences and their higher order harmonics and intermodulation products. The next term n_1' is the channel's noise contribution to the decision statistic and the final term q_1' represent the contribution of the quantization error to the correlation value.

The SNDR for the first symbol at the output of the correlator is defined as:

$$SNDR = \frac{s_1^2}{E[\sigma_{I_1'}^2] + \sigma_{n_1'}^2 + \sigma_{q_1'}^2} \tag{12}$$

The signal energy of the received UWB signal is

$$s_1^2 = N_c^2(\alpha_1 - \chi)^2 A_k^4 R_{ww}^2 \tag{13}$$

The distortion contribution at the output of the correlator is represented by the variance of I_1':

$$\sigma_{I_1'}^2 = E({I_1'}^2) = \alpha_1^2 A_k^2 \frac{l}{T_s} \sum_{i=1}^{\frac{l}{T_s}} R_{\xi\xi} \cdot R_{ww} \tag{14}$$

This variance value changes upon the hopping sequence c_j^k which is changed every symbol. Due to the non-static nature of $\sigma_{I_1'}^2$, the expected value of this variance is used in the SNDR calculation.

Since noise has a Gaussian distribution and each of the j^{th} chip's sampled noise is independent of each other, the variance of n_1' is computed as

$$\sigma_{n_1'}^2 = \frac{KTB}{2} N_c \alpha_1^2 A_k^2 R_{ww} \tag{15}$$

Finally, quantization noise is assumed Gaussian and uncorrelated with all other noise and interference terms. Therefore, ADC's quantization noise power equates to

$$\sigma_{q_1'}^2 = \frac{V_{lsb}}{12} N_c \alpha_1^2 A_k^2 R_{ww} \tag{16}$$

With the SNDR formulated, the BER can be calculated as:

$$BER = Q\left(\sqrt{\frac{s_1^2}{E[\sigma_{i_1'}^2] + \sigma_{n_1'}^2 + \sigma_{q_1'}^2}}\right) \tag{17}$$

Using (12)-(16), Monte-Carlo simulations were performed to obtain system SNDR. In the simulation environment, four 1.2 ns Gaussian doublets with a center frequency of 4 GHz and power spectral density (PSD) of -160 dBm/Hz were received per data symbol. Gaussian doublets with spacing of 4 ns, as proposed in [3], were employed to produce spectrum nulls to suppress interference and intermodulation distortion effects. The channel noise PSD was set by the $300K$ noise temperature and the 7 dB noise figure of the receiver frontend, which simulated an SNR of 13 dB in the absence of quantization error and non-linearity effects. Two external interferers residing in the 2.4 GHz ISM and 5 GHz UNII bands with -40 dBm power and random phase were also included. The RF pre-select filter contains a 3 to 4 GHZ 2^{nd} order bandpass filter and 2^{nd} order notch filters at 2.4 GHz and 5 GHz. Anti-alias baseband filter was modeled using 4^{th} order Butterworth filters. The simulated SNDR and the corresponding BER are plotted in Fig. 2 and Fig. 3 respectively.

It is seen in these figures that the performance of the system improves significantly with higher resolution ADCs. This demonstrates that a reasonable ADC precision is necessary to preserve the shape of the doublets and to cancel out interference effectively. Greatest performance improvements occur when the accuracy is increased from

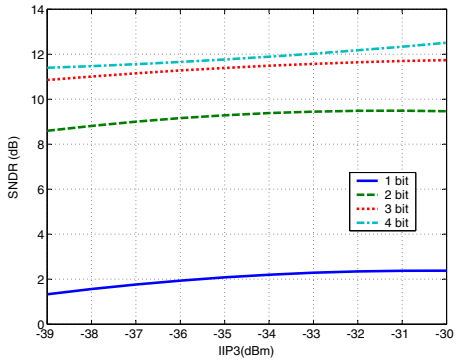


Figure 2: SNDR vs IIP3 for different ADC resolution

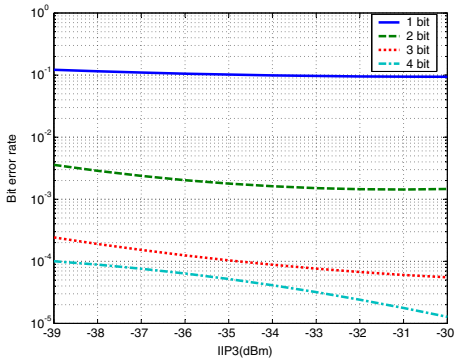


Figure 3: BER vs IIP3 for different ADC resolution

one to two bits. This BER improvement slowly diminishes with finer ADC resolution. The other trend that can be observed in the figures is that the BER is a decreasing function of IIP3 for all ADC resolutions. This can be explained by the system experiencing more benign intermodulation distortion and gain compression effects with a linear front-end. With low resolution ADCs, this trend is difficult to identify as the BER is dominated by quantization error. As the number of ADC bit increases, BER is no longer limited by the quantization error, and improvement from a linear front-end grows significantly. It should be noted that the negative effect of linearity on SNDR and BER can be reduced by stronger filtering functions prior to the LNA. Moreover, while the results obtained is specific to the conditions set in the simulation environment, the performance improvements due to increase in ADC resolution are similar to previous work, and hence applicable to pulse based UWB systems in general.

4. Hardware Power Estimation

In this section, we investigate the power-linearity trade-off in the RF front-end, followed by power analysis of the flash ADC architecture. The overall receiver power is estimated and the relationship between power, linearity and ADC precision analyzed.

4.1 RF Front-end Power Estimation

The receiver front-end shown in Fig. 1 consists of a LNA, a pair of mixers and a pair of baseband amplifiers, all of which operate with a 1.8V supply voltage. We start our analysis with MOS transistors, which is the main source of non-linearity in RF circuits and fundamental to the accurate analysis of front-end distortion.

4.1.1 Transistor Model and Nonlinear Coefficients

Continuous MOS transistor models presented in [11] provides good accuracy in both weak and moderate inversion regions, and the drain current I_d is given by

$$I_d = K \frac{X^2}{1 + \theta X} \tag{18}$$

where

$$X = 2\eta\phi_t ln\left(1 + e^{\frac{(V_{gs} - V_{th})}{(2\eta\phi_t)}}\right) \tag{19}$$

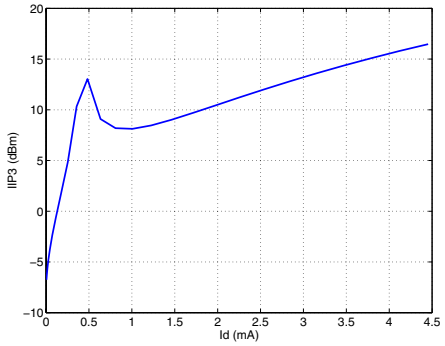


Figure 4: IIP3 vs I_d for a typical 0.18 μm CMOS process

In the equations above, K is a constant depending on the transistor size and the underlying technology and θ approximately models the combined mobility degradation and velocity saturation effects. Furthermore, $\phi_t = kT/q$ is the thermal voltage, V_{gs} is the gate-source voltage, V_{th} is the threshold voltage, while parameter η is related to the subthreshold factor and determines the rate of exponential increase of I_d with V_{gs} in the subthreshold region.

The drain current $i_d(v_{gs})$ of the CMOS transistor model above can be represented by a third order Taylor series expansion as

$$i_d(v_{gs}) = \alpha_1 v_{gs} + \alpha_2 v_{gs}^2 + \alpha_3 v_{gs}^3 + ... \tag{20}$$

where

$$\alpha_n = \frac{1}{n!}\frac{\partial^n I_d}{\partial^n V_{gs}}\bigg|_{V_{gs}=V_{GS}} \tag{21}$$

are the nonlinear coefficients. It can be seen that (20) is equivalent to (1) defined previously if we substitute v_{gs} for $x(t)$ and i_d for $Y(t)$ respectively.

From (18), (19), and (21), nonlinear coefficients can be derived according to [12] :

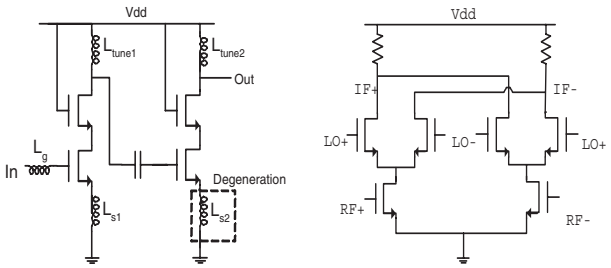
$$\alpha_1 = K\frac{X(2+\theta X)}{(1+\theta X)^2(1+s^{-2})} \tag{22}$$

$$\begin{aligned}\alpha_3 = {} & \frac{K}{6}\cdot\frac{-6\theta K}{(1+\theta X)^4}\left(\frac{1}{1+s^{-2}}\right)^3 \\ & + \frac{K}{6}\cdot\frac{-X(2+\theta X)}{(1+\theta X)^2}\cdot\frac{(s-s^{-1})}{(2\eta\phi_t)^2(s+s^{-1})^3} \\ & + \frac{1}{2}\left(K\frac{2}{(1+\theta X)^3}\cdot\frac{1}{2\eta\phi_t(1+s^{-2})(s+s^{-1})^2}\right)\end{aligned} \tag{23}$$

where $s = e^{(v_{gs}-v_{th}/(4\eta\phi_t))}$. By Setting $V_{gs} - V_{th}$ to 0.2 V and varying the device W/L ratio, (22), (23), (2), and typical $0.18\mu m$ CMOS parameters obtained from [13] can be utilized to derive the relationship between IIP3 and I_d. Fig. 4 shows a narrow peaking at I_d = 0.5mA. This linearity sweet spot is the subject of ongoing research [13]. The location of the peaking region, however, vary significantly with process variations, making operation in the sweet spot difficult to guarantee. Ignoring this narrow peaking, the plot shows a clear positive relationship between IIP_3 and I_d. Since these transistors are the fundamental building blocks of the RF front-end, this linearity power trade-off is common in all front-end circuitry, as will be evident in the subsequent sections.

4.1.2 *Low Noise Amplifier*

The LNA employs a stagger-tuned architecture shown in Fig. 5(a) to obtain flat gain in the 3 to 4 GHz range. Both gain stages are inductively degenerated common-source (CS) stages for input matching and improved linearity. Cascode transistors are included to improve isolation and prevent circuit instability. Closed form expressions for the third-order intermodulation distortion (IM3) of a degenerated cascode CS amplifier have been derived previously and



(a) Wideband LNA (b) Gilbert mixer

Figure 5: Front-end Circuits

interested readers are referred to [14] for detailed derivation. Using the calculated $IM3$, the $IIP3$ of a single amplifier stage can be computed as :

$$IIP3 = \sqrt{\frac{v_{in}^2}{IM3}} \tag{24}$$

In an N stage cascaded system where each stage j provide a gain of G_j, the overall IIP_3 can be expressed as follows [2]:

$$\frac{1}{IIP3_{tot}^2} = \frac{1}{IIP3_j^2} + \sum_{j=2}^{N}\left(\frac{1}{IIP3_j^2}\prod_{i=1}^{j-1}G_i^2\right) \tag{25}$$

Fig. 6(a) illustrates the power linearity relationship for a single CS gain stage, and the overall two-stage LNA. The first stage gain $G_1 = \alpha_1 \cdot |Z_L|$ is calculated with $|Z_L|$ set to 100 Ω . As expected, a trade-off between power and linearity can be observed. However, the delta improvement in overall IIP3 diminishes with increasing power due to the increasing gain in the first stage.

4.1.3 *Down-conversion Mixer*

One of the most popular down-conversion mixer topologies is the Gilbert cell shown in Fig. 5(b). This topology provides advantages such as high conversion gain and a high degree of isolation. We utilize the analytical expressions developed in [12] assuming a 4 GHz local oscillator (LO) with amplitude of 0.6 V. Note that only the low frequency effects are included in our analysis . This is valid because the capacitance effects at high frequency has minimal impact for LO drive of up to approximately 0.8V [12].

The switching pair's distortion behavior can be described by:

$$i_d = b_1 \cdot i_s + b_2 \cdot i_s^2 + b_3 \cdot i_s^3 \tag{26}$$

where

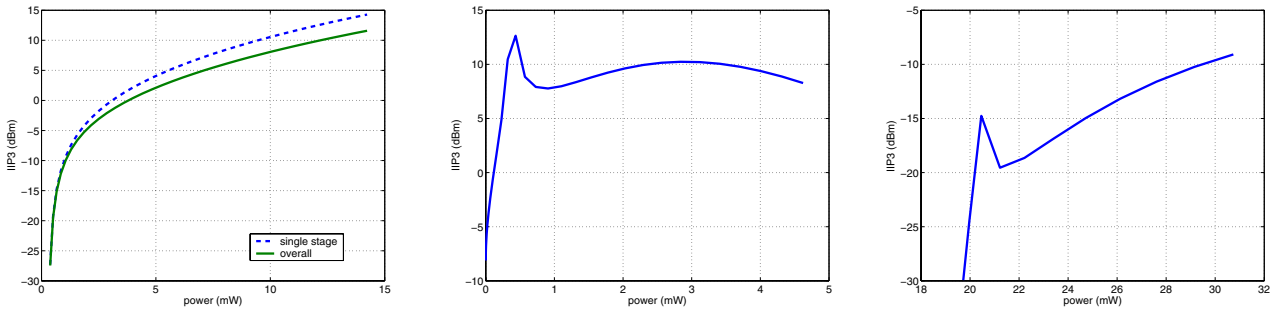
$$b_i = \frac{p_i, 1}{2} = \frac{1}{T_{LO}}\int_0^{T_{LO}} p_i(t) sin(2\pi f_{LO} t) \tag{27}$$

and $p_i(t)$ are the i^{th} order time-varying nonlinear coefficients that are functions of the bias current, LO voltage and the device characteristics.

After cascading the switching pair with the driver stage, the total mixer third-order intermodulation is approximated by

$$IM3_{mixer} \approx \frac{3}{4}\left(\frac{a_3}{a_1}V_{in}^2 + \frac{b_3}{b_1}a_1^2 V_{in}^2\right) \tag{28}$$

where a_3 and a_1 are the nonlinear coefficients of the driver stage. Using (24) and (26) - (28), IIP3 of the mixer is estimated and shown in Fig. 6(b). The plot indicates linearity improvement with increasing power for power levels below approximately 3 mW. Beyond that point, linearity decreases with increasing power. This is a direct result of the combined action of the driver and the switching transistors. In the low power region, linearity improvements of the driver transistor dominate. As the biasing power continues to increase, the existing level of LO drive is no longer sufficient to maintain reliable switching, resulting in linearity degradation.



(a) Wideband LNA (b) Gilbert mixer (c) Differential CS amplifier

Figure 6: IIP3 vs power

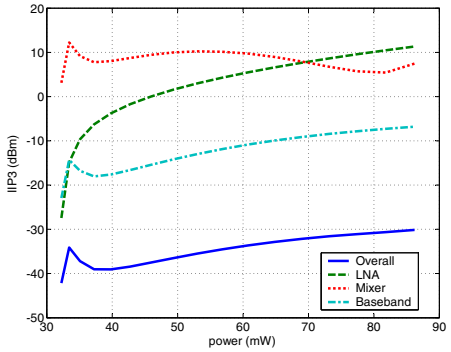


Figure 7: IIP3 vs power for RF front-end

4.1.4 Baseband Amplifier

The baseband amplifier block is configured as four cascaded stages of differential pair configuration. Complex negative feedback networks are avoided in order to maximize bandwidth and alleviate potential for circuit instability. In order to desensitize the overall amplifier's linearity from the gain in the first three stages, only the last stage's biasing power was varied. This ensures linearity improvements with increasing power consumption.

Using [15], the third order harmonic distortion (HD3) of a single stage differential CS amplifier can be expressed as

$$HD3_{diff} \approx \frac{v_{in}^2}{32(v_{gs} - v_{th})^2} \tag{29}$$

and the IIP3 of a single stage is

$$IIP3_{diff} = \sqrt{\frac{v_{in}^2}{3HD3}} \tag{30}$$

The overall IIP3 of the four-stage amplifier is then obtained via (30), (25) and shown in Fig. 6(c)

4.1.5 Overall Front-end

By treating the receiver as a cascaded system consisting of the LNA, mixer and baseband amplifier, the overall front-end linearity is predicted with (25). The LNA gain $G_{LNA} = \alpha_1 \cdot |Z_L|$ is calculated with $|Z_L|$ set to 1.5k Ω. The mixer's load resistance R_L is set to 200 Ω for calculating G_{mixer}. The IIP3 of the individual blocks and the overall front-end is plotted against total front-end power budget in Fig. 7. As expected in a cascaded system, the overall linearity is mainly restricted by the linearity of the last stage (baseband amplifier) and the gain of the previous stages (LNA and mixer). Approximately 10 dB enhancement in linearity can be observed when the power increases from 30 mW to 85 mW. With additional power dissipation, gain in the LNA and mixer stages increases, resulting in gradual compression of the overall linearity. This effect is demonstrated by the diminishing linearity improvements in the high power region when compared to the low power region.

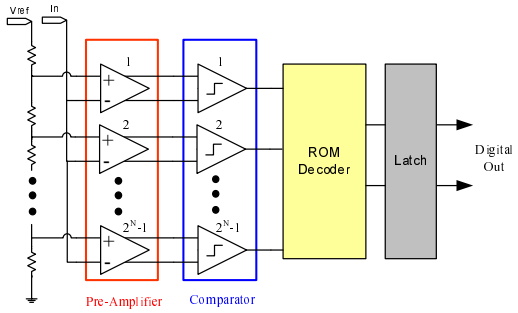


Figure 8: N bit flash converter architecture

4.2 ADC power estimation

As is generally known, flash ADCs are well suited to high speed, low resolution applications [16]. Fig. 8 shows the block diagram of an N bit flash converter which consists of a reference ladder and analog pre-amplifiers, followed by high speed digital comparators and decoding circuitry. The reference ladder subdivides the divider reference voltage in a set of $2^N - 1$ reference voltages, which are compared with the analog input signal in parallel and converted to a binary code. For the purpose of estimating the power usage, the pre-amplifier and comparator stages are examined.

The analog pre-amplifier often assumes a differential pair structure to provide gain and minimize the effect of kickback noise from the subsequent comparator stage [6]. In the power estimation, it is assumed that the pre-amplifier used for a single bit is biased with I_d of 250μA. A factor of four increase in power for every bit increase in ADC accuracy is necessary because of device matching considerations [17], yielding the following expression for the power of the pre-amplifier:

$$P_{preamp} = (2^{2N} - 1) \cdot V_{dd} \cdot I_d \tag{31}$$

Estimation of the digital comparator array's power have been formulated in [18] and [19]. Comparisons between the two work with published ADCs found [18] to be more accurate for integrated ADCs, and its power estimation formula is:

$$P_{comp} = \frac{\alpha \cdot V_{dd} - \beta \cdot V_{swing}}{\eta} \cdot V_{dd} \cdot L_{min} \cdot f_{sample} \tag{32}$$

where $\alpha = 0.5$, $\beta = 0.3$, and $\eta = 32.1$ x 10^3 are empirical coefficients found in [18]. L_{min} is the effective transistor length, f_{sample} = 2 GHz is the sampling speed and $ENOB$ is the effective number of bits. In practice, an ADC's ENOB deviates slightly from the number of bits in the ADC specification due to implementation loss. Therefore, N can be substituted for $ENOB$ with sufficient accuracy for power estimation purposes. Summation of the comparator and pre-amplifier power produces the total power for each of the ADCs in the I and Q streams of the receiver. Multiplying by two will produce the overall ADC power as shown in Fig. 9

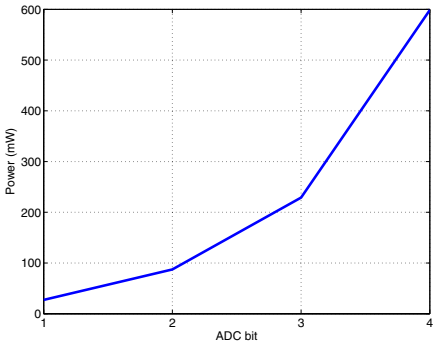


Figure 9: Total ADC power consumption

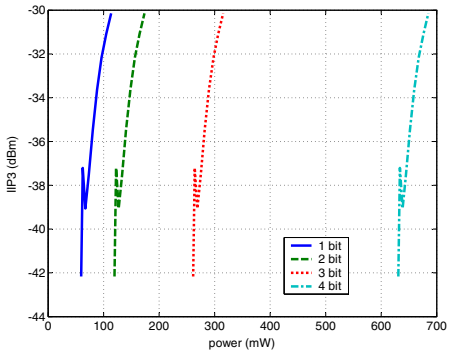


Figure 10: Complete receiver power consumption

4.3 Overall Receiver Power Estimation

The complete receiver power for different ADC resolutions and front-end linearity is shown in Fig. 10 and demonstrates that the ADC's power dissipation is substantial even with only one or two bit accuracy. Further improvements in the ADC accuracy increase the power usage beyond 200 mW, dominating the overall receiver power.

5. Power and Performance Analysis

In this section, the results obtained in section 3 and section 4 are summarized to investigate the trade-off between linearity and ADC accuracy with regards to their effects on system BER and power budget. Shown in Fig. 11 is the power consumption plotted against BER performance for all possible configurations in the design space. From this graph, suitable architectural choices can be made based on the specific constraints of particular applications. For applications such as a high speed wireless home theater, where high quality of service must be maintained, three or four bit ADCs are necessary. In contrast, a low rate, battery operated sensor can tolerate higher BER in exchange for lower power dissipation and extended battery life.

The Pareto optimum points illustrate the best configurations for any given combination of power consumption and BER performance. Close examination of these Pareto points reveal that linearity are less important for receivers employing low resolution ADCs, as evidenced by the fact that a sublinear front-end with two bit ADC is more optimal than a linear front-end with one bit ADC. However, linearity is more critical when used in conjunction with higher resolution ADCs. The Pareto points clearly indicate that a linear front-end with three bit ADCs is more power efficient than a sublinear front-end with four bit ADCs. The reason behind these observations are two fold. Firstly, higher ADC resolutions result in diminishing BER reduction and exponential increase in power consumption. In the mean time, more accurate ADCs reduce the quantization error, and the effect of front-end linearity on BER are more pronounced. Therefore, with high resolution ADCs, improving front-end linearity is a more power effective solution to reducing the BER.

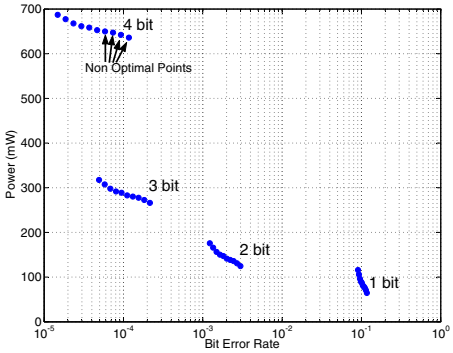


Figure 11: Full design space

6. Conclusion

In this paper, the performance of digital DS-UWB systems operating with sublinear analog front-ends are evaluated. The simulation results show that a minimum ADC resolution of two bits is necessary to obtain a reasonable BER in the presence of interference and intermodulation distortion. Front-end linearity becomes increasingly critical for three or more bits of precision. Analysis of the hardware power dissipation is included and combined with BER performance to derive the optimal circuit configurations. It is shown that tradeoffs in front-end linearity and ADC precision exist and can be utilized to optimize system reliability and power consumption.

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