2019 COMP3222 Lab 4 Notes and Additional Questions

The COMP3222 teaching staff have concluded some tweaks are needed to improve the learning outcomes from labs. For this lab, as well as for the remaining future labs, we will publish additional guidance as we see fit and explain in more detail what we will be looking for.

In addition to the 3 marks for successfully completing parts 1, 2 and 4 of Lab 4, we will
- award up to ONE mark for your paper design of PART 4, and
- award up to ONE mark for your coding style.
How these marks will be awarded is detailed below.

Part 1
- HINT: use a GENERATE statement – refer to L04/S43-S44

Part 2
- Explain the difference in Fmax between the 8- and 16-bit versions of the counters (Parts 1 & 2)?

Part 4
Prior to implementing your counter you should prepare an outline of your design on paper. This design is worth up to ONE mark. In the future, please note that if you do not show a requested paper-based design, you will not be given any marks for the part of the lab associated with the design.

For this part of the lab, you are required to prepare a so-called block diagram of your design that includes the interconnection of three components:
  1. A one-second timer with asynchronous clear. This timer, which is controlled by a 50MHz clock signal, outputs a pulse for one clock period every second.
  2. A BCD-counter with enable and asynchronous clear. You should design, implement and simulate this component before connecting it to the one-second timer.
  3. The 7-segment display from Lab 3, part 5 or L04/S33.
Your diagram should include the connections of the circuit to the resources provided by the DE1 board.

Coding style
Apart from correctness, the guiding principle for code style in COMP3222 is understandability and maintainability. Up to ONE mark will be awarded for your coding style on all three parts of the lab. Points to be taken into account include:
- Proper indentation
- Use of meaningful names for entities, architectures, signals and labels
- Alignment between your block diagram for part 4 and your code
- Correct VHDL use
- Appropriate decomposition of a design into sub-components
- Adherence to the lab specifications