The ARM Architecture

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Introduction

ARM – a 32-bit RISC processor architecture

- ARM licenses
  - Implementation license
    - Hard cores
    - Soft cores
  - Architecture license

ARM features

- ARM features
  - simple
  - cheap
  - low-power
  - modular
  - high-performance

	Frequency	Power	Performance
PXA255	400MHz	0.3w	480MIPS
Pentium 2	300MHz	14w	477MIPS

History

BBC micro

ARM Version 1:
- ARM1 by Acorn Computers – the 1st commercial RISC processor

History

Archimedes

ARM Version 2:
- Coprocessor support
- On-chip cache

Cores:
- ARM2, ARM3

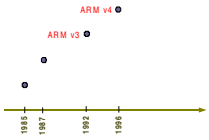
History

Apple Newton

ARM Version 3:
- 32-bit
- MMU
- Coprocessor emulation
- 64-bit MAC

Cores:
- ARM 6, ARM 7 (by ARM Ltd)

History

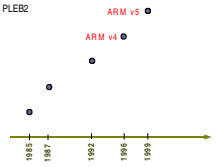


ARM Version 4:
- Thumb

Cores:
- ARM7TDMI, ARM8, StrongARM, ARM9TDMI

History

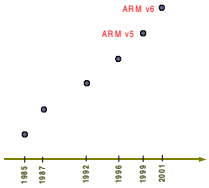
PLEB2



ARM Version 5:
- DSP extension
- Jazelle

Cores:
- ARM10TDMI, XScale

History



ARM Version 6:
- Thumb-2
- TrustZone
- SIMD extension

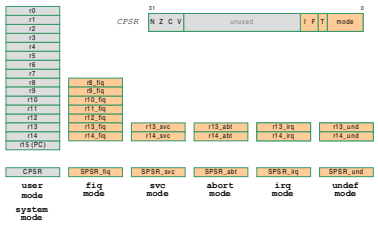
Cores:
- ARM11xxx, ARM11 MPCore

The ARM ISA

ISA overview

- RISC features:
  - Load-store architecture
  - Fixed-length 32-bit instructions
  - 3-address instruction format
  - Large register bank
- But:
  - No register windows
  - Multiple-cycle instructions

Registers



Types of instructions

- Data processing instructions
- Data transfer instructions
- Control flow instructions

Data processing instructions

- Addition, subtraction, multiplication, comparison, bitwise ops
- Multiply-accumulate
- Two 32-bit operands, 32/64-bit result
- Second operand can be register or immediate
- Second operand can be shifted or rotated
- Optional modification of condition codes

Data transfer instructions

- 4/2/1-byte load/store
  - base + offset addressing
  - auto-indexing

```
LDR r0, [r1,#4]!
```

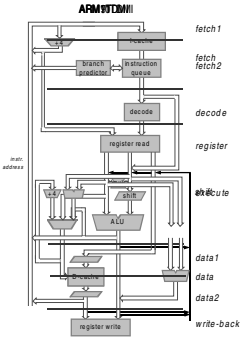
- Multiple register transfer
  - load/store up to 16 registers
  - auto-indexing

```
LDMIA r0!, {r2-r9}
```


Control flow instructions

- Unconditional & conditional branches
- Conditional execution
- Branch and link

ARM Pipeline Evolution



Exceptions

- Reset
- Data abort
- FIQ
- IRQ
- Prefetch abort
- Supervisor call (SWI); undefined instruction

Coprocessors

- Up to 16 co-processors
  - up to 16 registers per coprocessor
  - load-store architecture
- Coprocessor instructions
  - data processing (internal to coprocessor)
  - load-store (controlled by ARM)
  - register transfer

Memory System

Cache

- Cache organisation
  - separate instruction and data cache
  - virtually addressed
  - set-associative
  - copy-back
  - cache lock-down capability

Protection

- Closed systems
  - protection unit
    - no address translation
    - 8 regions
- General-purpose systems
  - memory management unit

Memory management unit

- 2-level page table
  - 1M, 64K, 16K, 4K, 1K pages
  - no-access/read-only/read-write protection
- Separate instruction and data TLBs

Context switches

- Page table switch cost
  - TLB flush
  - cache purge
  - TLB & cache reload
- Protection domains
  - 16 domains
  - manager/client/no-access protection scheme
- Fast context switch extension
  - 128x32M process blocks

ISA extensions

- Thumb
- Jazelle
- SIMD